LEARNING MATERIAL ON

ANALOG ELECTRONICS & OPAMP

DEPARTMENT OF ELECTRICAL ENGINEERING

GOVERNMENT POLYTECHNIC KORAPUT

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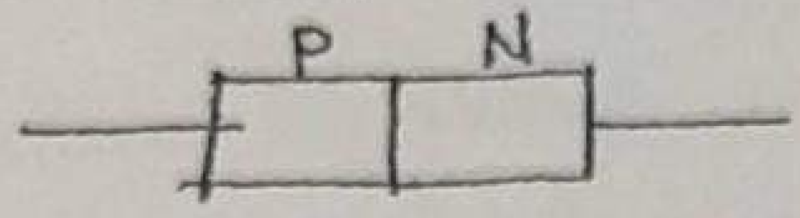
PN Junction diode: Analog

By combining P-type & N-type semiconductor we get PN Junction diode



P-type semi-conductor:

P-type → Intrinsic semiconductor + III group

IV group atoms

[pureform of semi conductor]

Ex: Boron, Aluminium, Gallium, Indium are Trivalent. (3 valence $\bar{e}$)

Ex:
Carbon
* Silicon (Best) *
Germanium
Tin
Lead

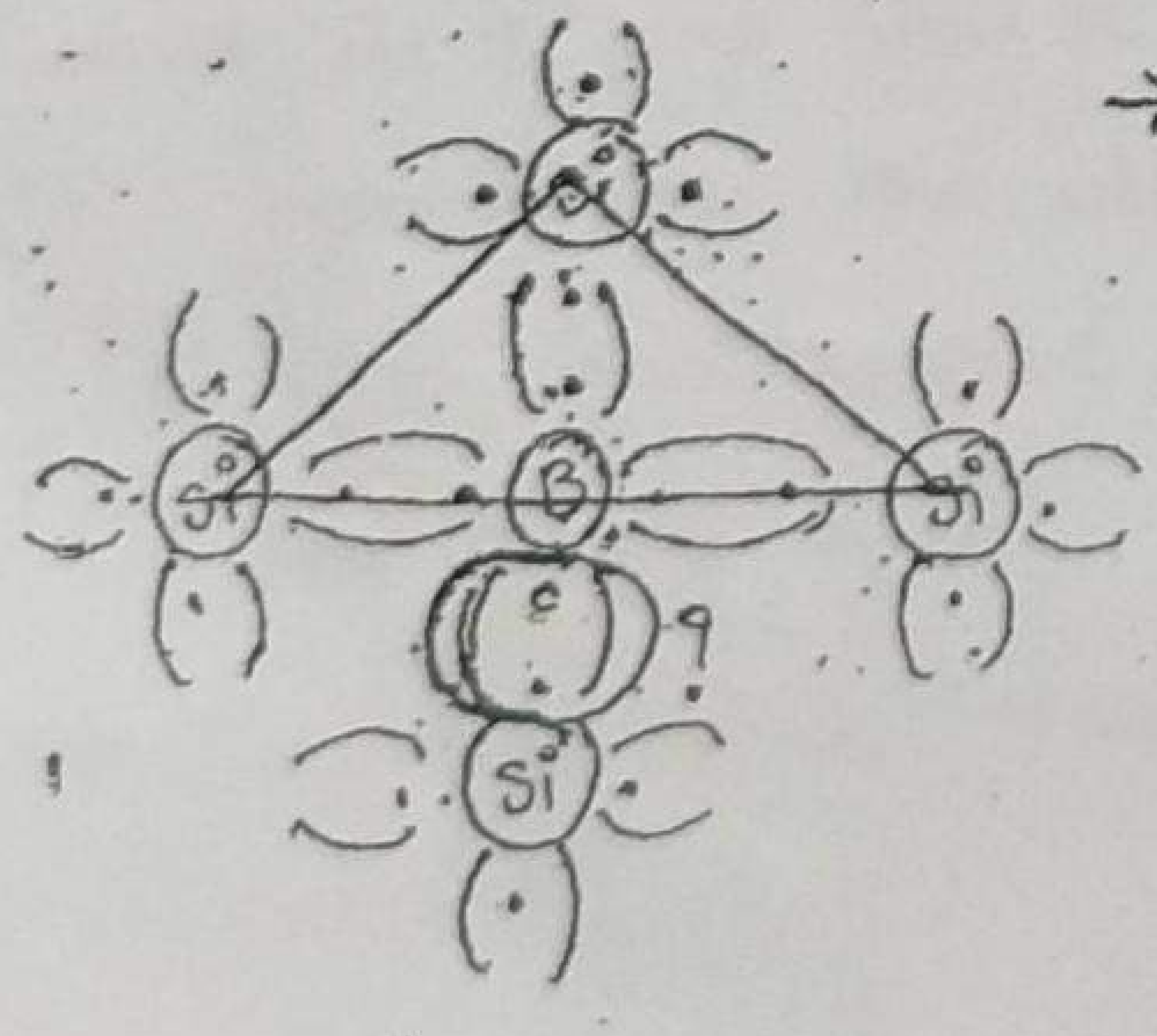
(4 valence $\bar{e}$)

why?

* Si, Ge → considered as semiconductor as these two are abundant and provide moderate values of current and voltage.
* Si is more availability.
* Thermal stable is more with Si.

$$\underset{0.7}{\underline{\text{cut in Vol}}}_{Si} > \underset{0.3}{\underline{\text{cut in Vol}}}_{Ge}$$

* I/p noise [due to humming] is less.



→ The 3 valence $\bar{e}$ of Boron forms 3 covalent bonds with the 3 nearest 'Si' or 'Ge' atoms. There is no $\bar{e}$ in the 4th covalent bond. There is a missing of $\bar{e}$ in This is considered as hole.

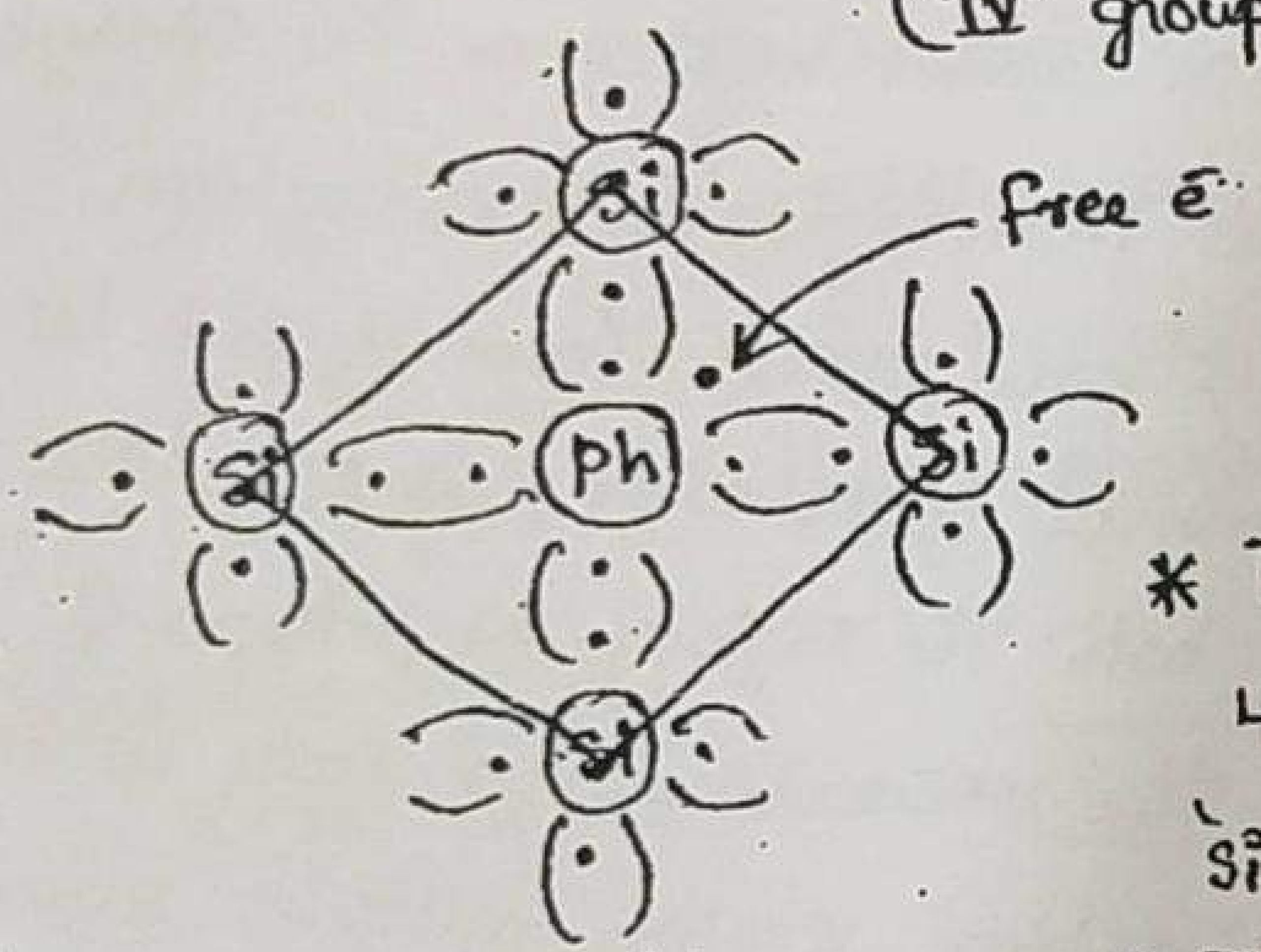
→ each atom of 3rd group provides one hole. In p-type semi conductor → Majority carriers → holes
minority carriers → $\bar{e}$

→ The 3^{rd} group atom is always ready to accept an $\bar{e}$. The 3^{rd} group atoms are also called as Acceptor atoms.
After accepting an $\bar{e}$, it becomes Negative ion (or) acceptor ion and is represented by ⊖.

N-type semi conductor :-

N-type → Intrinsic semi conductor + V group
(IV group atoms)

Ex: phosphorous, Arsenic, Antimony, Bismuth } pentavalent elements (5 valence $\bar{e}$)



* The 4 valence $\bar{e}$ of phosphorous forms 4 covalent bonds with the '4' nearest 'Si' (or) 'Ge' atoms.
* The 5th valence $\bar{e}$ of phosphorous is free each atom of V group provides one free $\bar{e}$.

* In N-type semi conductor → Maj carriers → $\bar{e}$
Minority " → holes.

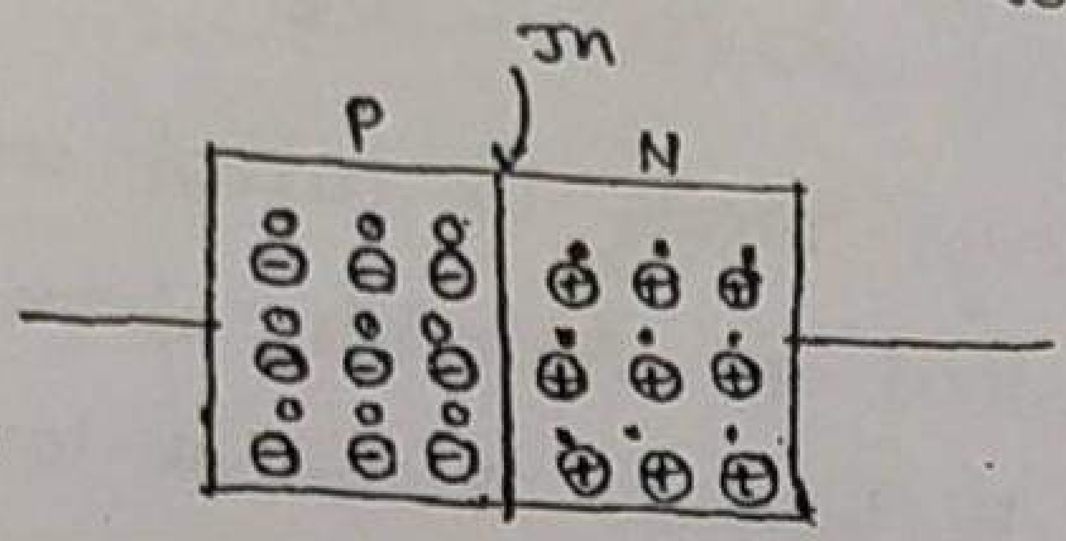
* The 5^{th} group atom is always ready to donate an $\bar{e}$. The V group atoms are also called as Donor atoms.
* After donating an $\bar{e}$, it becomes +ve ion (or) donor ion and is represented by ⊕.

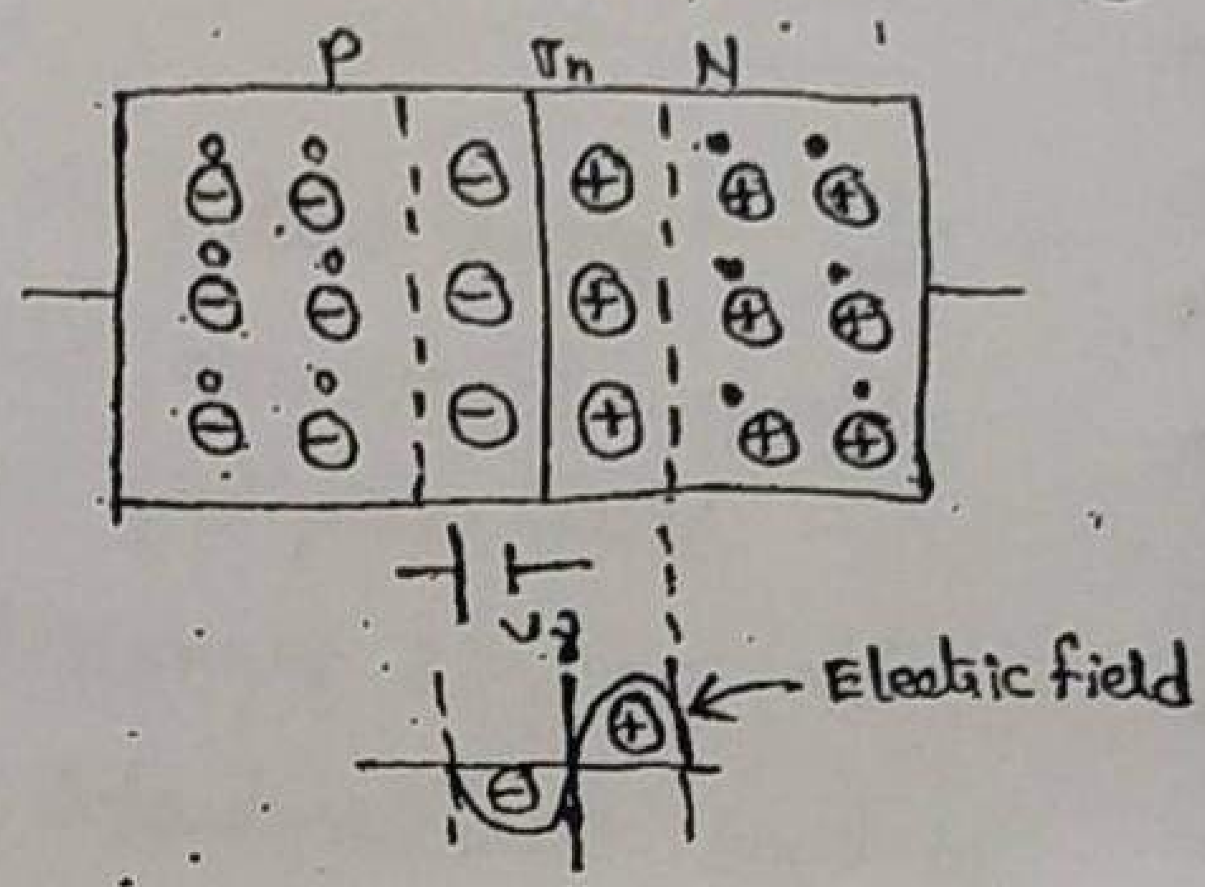
→ The layer which seperates p-type & N-type semiconductors is called Junction.

Doping levels $1 : 10^8$
1 → Doped atoms
10^8 → Intrinsic atoms.

→ p-type & N-types are equally doped.

→ The PN Junction diode is also called "Homo Junction device"





→ By combining p-type & N-type semiconductors a small force acting on the Junction. This force causes motion in the charged particles, These charged particles from higher concentration to lower concentration ie electrons moves from N-side to P-side & holes moves from p-side to N-side. Due to this recombination takes place in both the regions as p-type & N-type are equally doped, the recombination rate is same in both the regions. The depletion region width is same in p-type & N-type regions. The region in which there is no availability of charged particles is called <u>depletion region</u> (or) <u>Barrier</u> (or) <u>space charge region</u>.

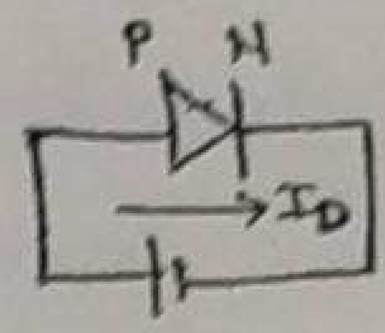
→ The induced voltage across the Junction is called depletion region voltage (or) Barrier voltage (or) space charge region voltage (or) cut in voltage (V_γ).

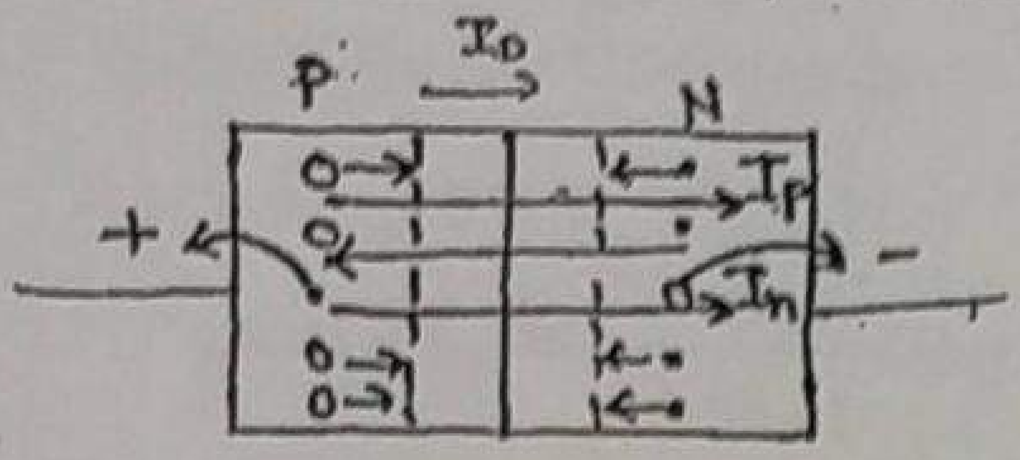
$$V_\gamma = \begin{cases} 0.7V \rightarrow Si \\ 0.3V \rightarrow Ge \end{cases}$$

Scanned by TapScanner

1.2 Working of Diode
1.3 V-I characteristic of PN junction Diode.

Forward bias of a PN Junction diode:-





* All the minority carriers of p-type & N-type moves away from Junction. They cannot form loop $\boxed{I_{min} = 0}$

→ The majority carriers of p-type & N-type moves towards the Junction. $\boxed{I_D = I_p + I_n}$

As F.B voltage(V)↑:- The repelling forces to the majority carriers Increases. * Depletion region width ↓
* Junction resistance ↓

→ AS V↑↑ depletion region width ↓↓
when $V = V_\gamma$, the depletion region width reduced to zero. The charged particles start crossing the Junction.

(i) when $V < V_\gamma$:
These exists barrier $\boxed{I_0 = 0}$

(ii) when $V = V_\gamma$:- This is min voltage to make depletion region width zero, the charged particles starts crossing the Junction.

$\boxed{I_0 \neq 0}$.

→ The current through the diode at this potential is called "SIGNIFICANT CURRENT" (Atleast 1% of max diode current)

(iii) when $V > V_\gamma$
The no. of charged particles crossing the Junction Increases. The current through the diode increases nonlinearly (or) exponentially and is given by

$$\boxed{I_D = I_0 \left[e^{V_D/\eta V_T} - 1 \right]}$$

I_0 - Reverse saturation current
V_D - voltage across F.B diode
η → Ideality factor whose value depends on type of material
$\eta = \{ 1 \rightarrow Ge$

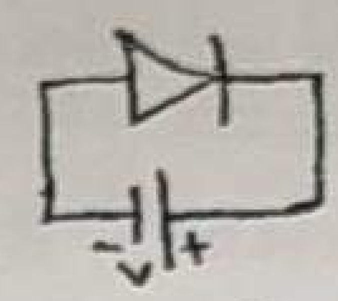
V_T - Temperature dependent voltage

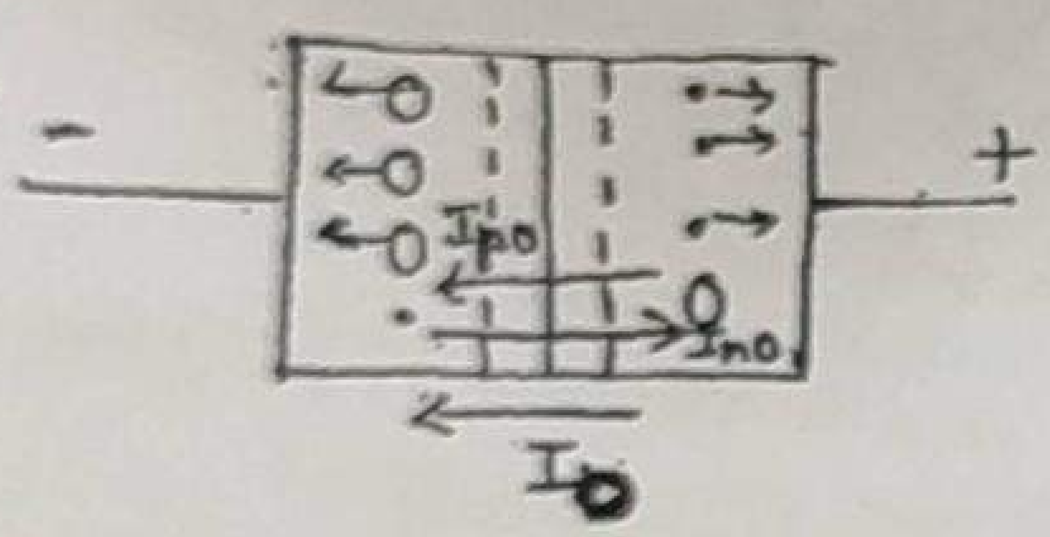
$$V_T = \frac{KT}{q} = \frac{T \leftarrow {}^\circ K}{11{,}600}$$

At Room temp, $T = 300^\circ K$ $\quad V_T = \frac{300}{11{,}600} \simeq 26\,mV.$

→ The applied voltage across the diode in such a way that, that makes the conduction of current in the direction of arrow head is called forward biasing.

Reverse bias of PN Junction diode:-





* All the majority carriers are moving away from Junction. They cannot from loop $\boxed{I_{majority} = 0}$

* The minority carriers moves towards the Junction.

AS R.B Voltage ↑ :-

* The majority carries move rapidly attracted by their respective terminal voltages i.e more rapidly move away from Junction.
  - → Depletion region width ↑.
  - → Junction resistance ↑.
  - → Junction temp ↑.

AS V↑↑, ~~b/c~~ Dep. region width↑↑

Temp across Junction ↑↑, Hence

* The minority carriers crossing the Junction ↑.

AS T↑, Breakge of covalent Bond ↑

$\bar{e}$-hole pairs are generalised ↑, Hence

* The no. of minority carriers crossing the Jun ↑.

$$\boxed{I_0 = I_{no} + I_{po}}$$

This I_0 flows from N-type to p-type i.e reverse to the direction of arrow head 'I_0' → Reverse current.

The Reverse current at Room temperature is called reverse Saturation current.

As V↑↑, T↑↑, I_o↑↑

At some particular voltage, temp across the Junction becomes max. This temp permanently damages the PN Junction diode.

→ This voltage is called "BREAK DOWN VOLTAGE" (≃30V).

As T↑, I_o↑

for every 1°c rise in temp I_o↑ by 7%.

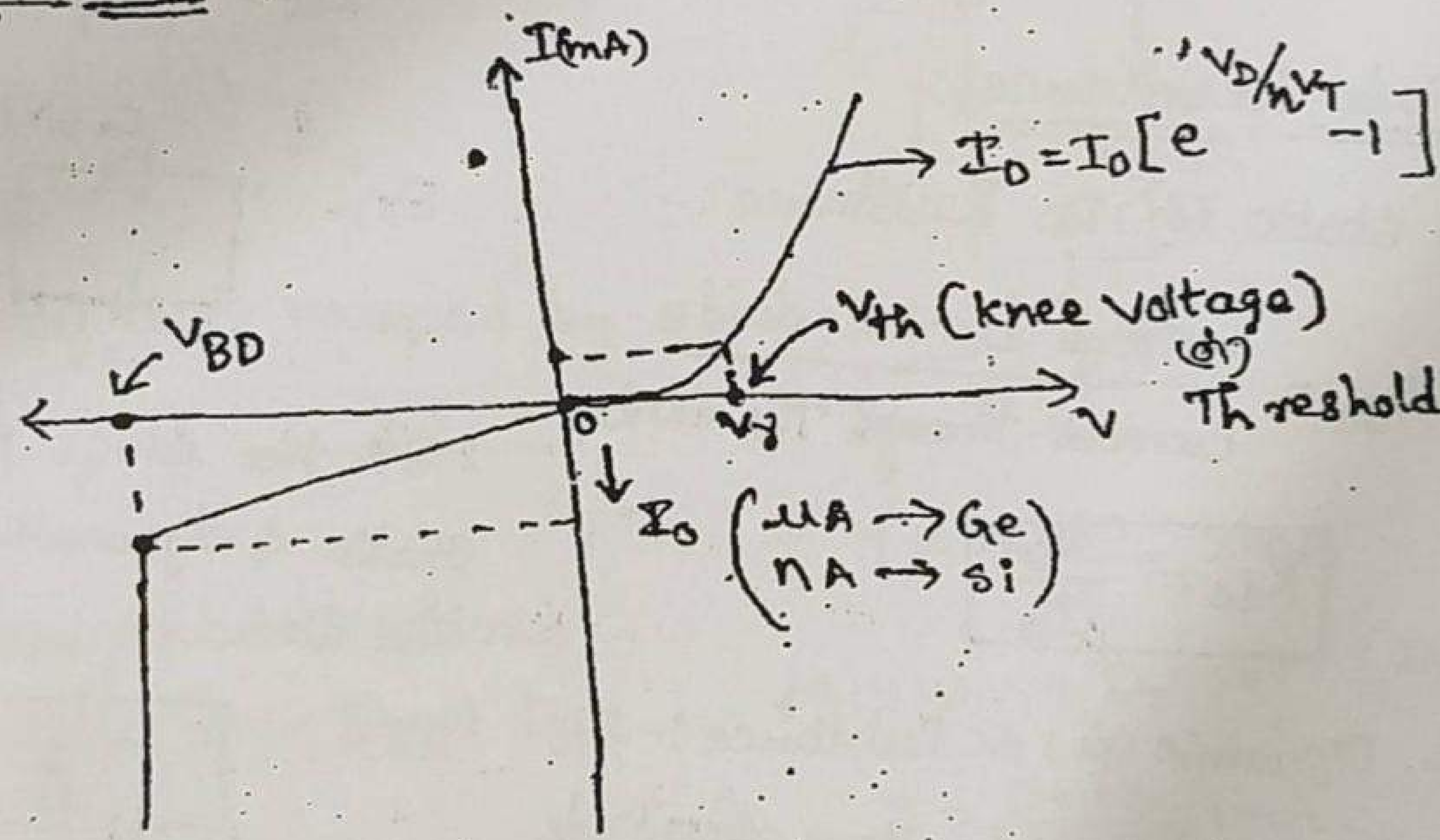
for every 10°c ↑ in temp, I_o Doubles

$T_1°C \rightarrow I_{o1}$

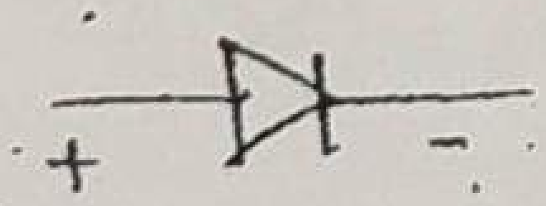
$T_2°C \rightarrow I_{o2}$

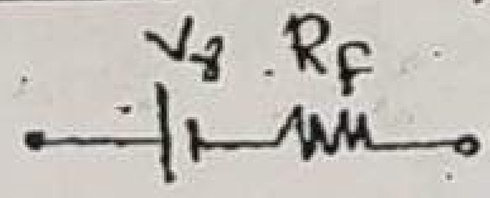
$$\therefore \boxed{I_{o2} = I_{o1}\, 2^{\left(\frac{T_2-T_1}{10}\right)}}$$

Characteristics:-

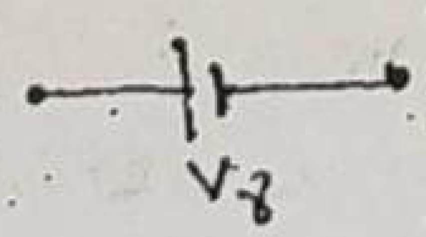


Diode equivalent circuit:-

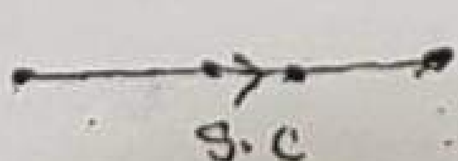
f.b. 

⇒ 

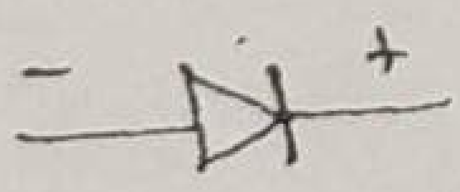
(when V_γ & R_f both given)

⇒ 

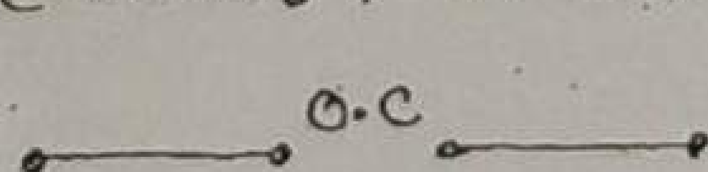
(when only V_γ given i.e $R_f=0$)

⇒ 

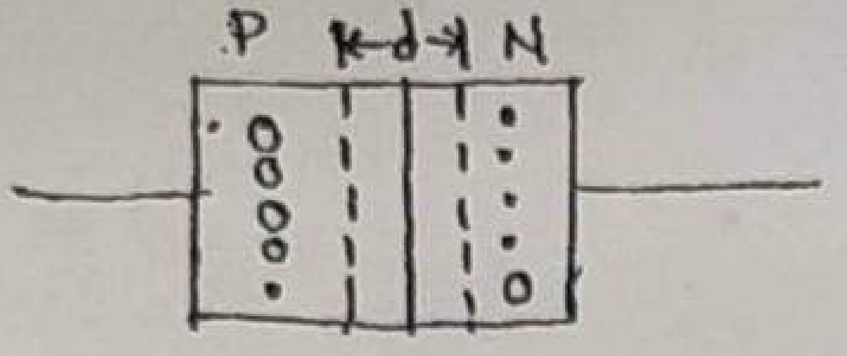
(when $V_\gamma=0$ & $R_f=0$ (or) Diode is IDEAL)

R.B 

* when diode R.B it conducts the currents in the order of μA (Ge diode), nA (Si). These currents are insignificant.



Diode capacitances:-



$\therefore C = \frac{\epsilon A}{d}$.

Diode offers:- AB$\boxed{C}$E$\boxed{F}$ (opp) PQ$\boxed{R}$S$\boxed{T}$ (opp)

(i) $\boxed{D}$iffusion capacitance $[C_D]$
— under $\boxed{F}$orward bias

(ii) $\boxed{T}$ransition capacitance $[C_T]$
— under $\boxed{R}$everse bias

→ As F.B voltage ↑ d↓ C_D ↑.

→ As R.B voltage ↑ d ↑ C_T ↓.

Diode Resistances:-

1. Static (or) DC Resistance :-

$$R_{dc} = \frac{\text{Voltage across diode}}{\text{Current through the diode}}$$

$$\boxed{R_{dc} = \frac{V_D}{I_D}}$$

2. Dynamic (or) AC Resistance :-

$$R_{ac} = \frac{\text{change in voltage across diode}}{\text{change in current through the diode}}$$

$$\boxed{R_{ac} = \frac{\Delta V_D}{\Delta I_D} \text{ (or) } \frac{dV_D}{dI_D}}$$

$$\therefore R_{ac} = \frac{\eta V_T}{I_D}$$

→ when the diode is F.B, it follows the current eq.

$$I_D = I_0\left[e^{V_D/\eta V_T} - 1\right]$$

$$I_D = I_0 e^{V_D/\eta V_T} - I_0$$

$$I_D + I_0 = I_0 e^{V_D/\eta V_T}$$

$$I_D >> I_0 \Rightarrow I_D + I_0 \simeq I_D.$$

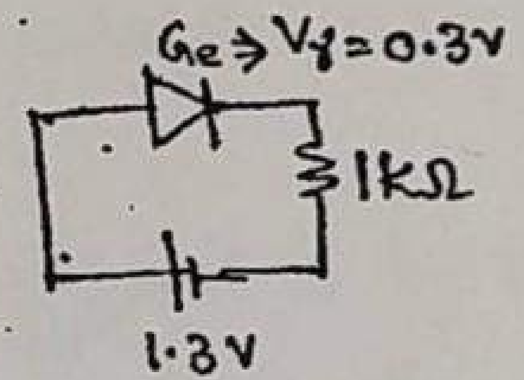
$$\boxed{\therefore I_D \simeq I_0 e^{V_D/\eta V_T}}$$

Diff w.r.t V_D

$$\frac{dI_D}{dV_D} = \underbrace{I_0 \cdot e^{V_D/\eta V_T}}_{I_D}\left(\frac{1}{\eta V_T}\right)$$

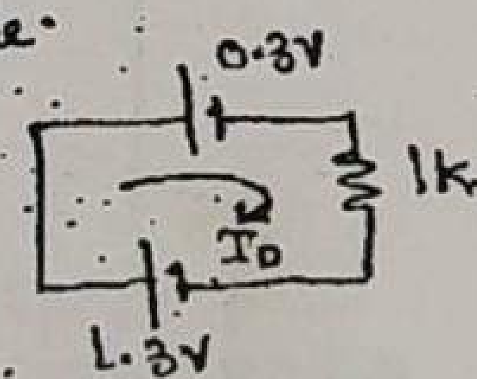
$$\frac{1}{R_{ac}} = \frac{I_D}{\eta V_T} \Rightarrow \boxed{R_{ac} = \frac{\eta V_T}{I_D}}$$

Ex:-



for the diode ckt shown, find the static & dynamic resistances of the Ge diode.

Sol:-



$$I_D = \frac{1.3 - 0.3}{1K} = 1mA$$

$$R_{DC} = \frac{V_D}{I_D} = \frac{0.3}{1mA} = 300\Omega$$

$$R_{ac} = \frac{\eta V_T}{I_D} = \frac{1 \times 26 \times 10^{-3}}{10^{-3}} = 26\Omega$$

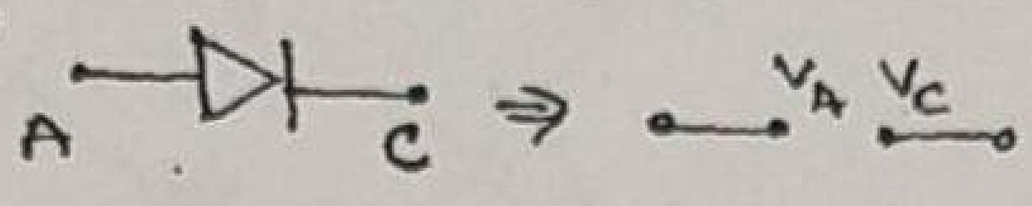
($\eta = 1$ for Ge)

($V_T = 26mV$ for room temp)

O.C & S.C Tests for diode Ckts:-

O.C Test:-

- "All the diodes are replaced by O.C"



* calculate $(V_A - V_C)$ for each diode

If $(V_A - V_C) > V_\gamma \rightarrow$ Diode - ON

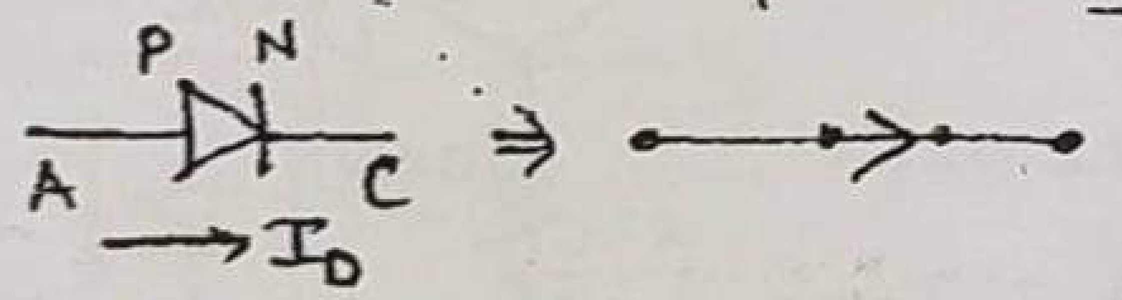
$(V_A - V_C) \leq V_\gamma \rightarrow$ Diode - OFF

* when no. of diodes having $(V_A - V_C) > V_\gamma$, the diode which has more $(V_A - V_C)$ becomes ON First.

* Again calculate $(V_A - V_C)$ for remaining diodes.

S.C Test:-

- "All the diodes are replaced by S.C"



Assume the current directions through each diode from P to N type only.

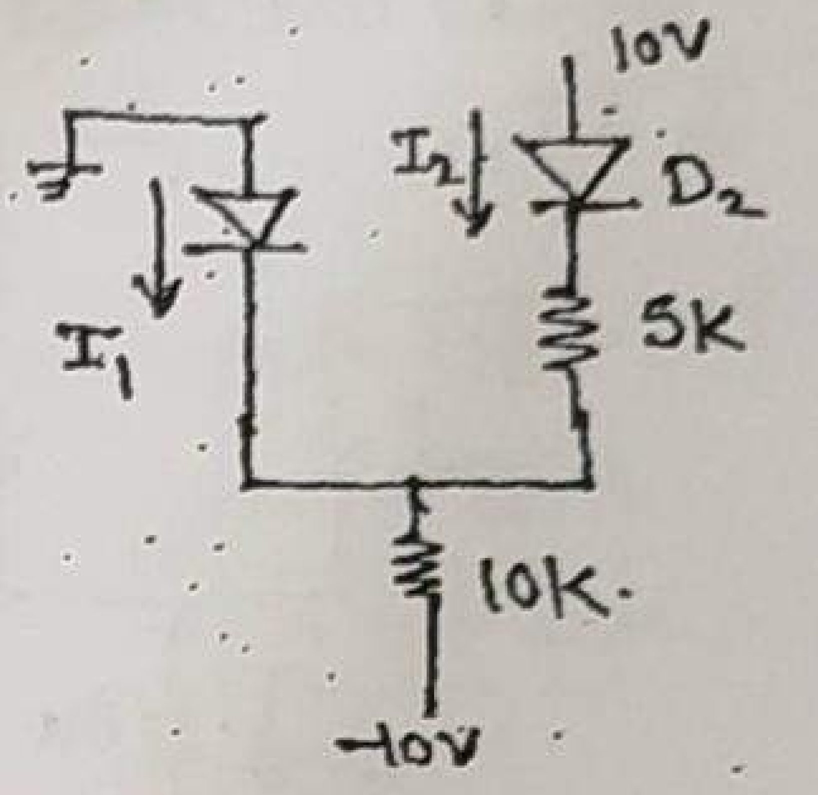
calculate the current through each diode.

If $I_D > 0 \rightarrow$ 'D' - ON

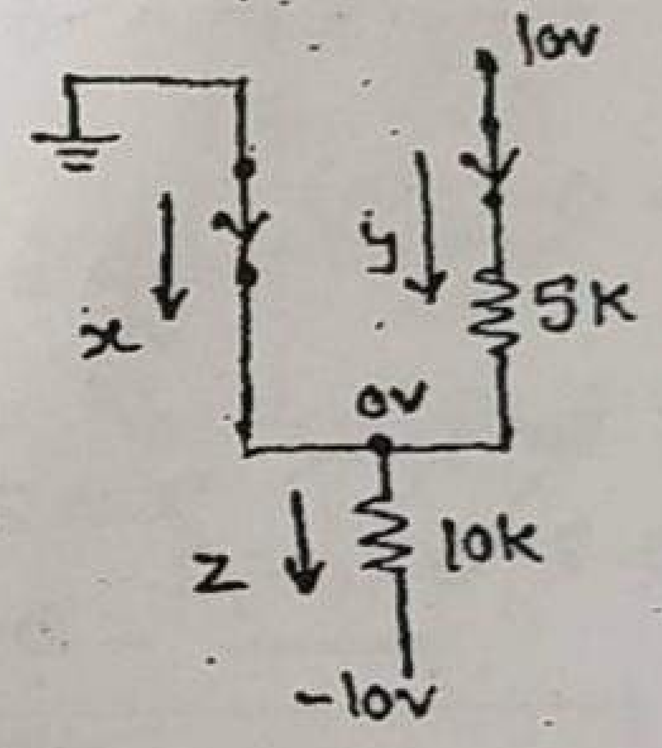
$I_D \leq 0 \rightarrow$ 'D' - OFF

problems:

Pb:- For the diode ckt shown, calculate the currents I_1 & I_2, assume that diodes are ideal



Sol:- (i) D_1 & D_2 are replaced by S.C



$$y = \frac{10-0}{5K} = 2mA$$

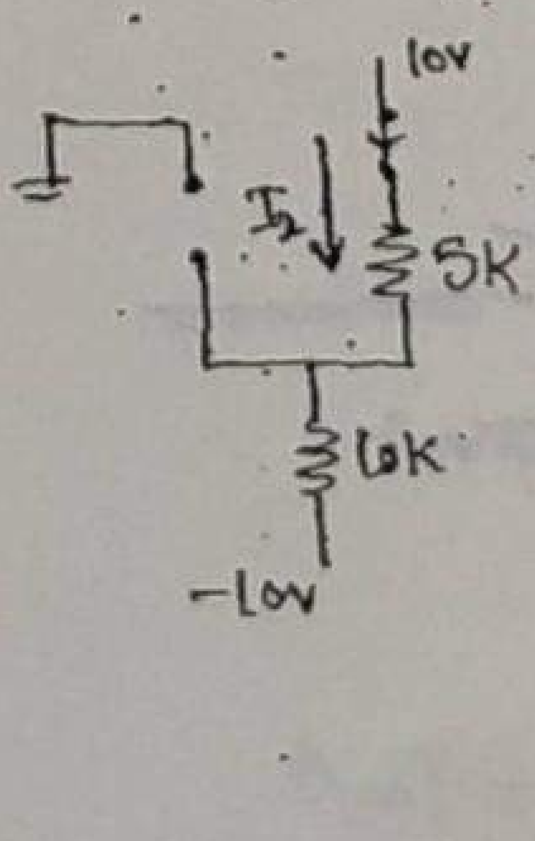
As $y > 0 \Rightarrow D_2$ - ON (Assumption Correct).

$$Z = \frac{0+10}{10K} = 1mA$$

$$Z = x + y \Rightarrow x = Z - y$$
$$= 1mA - 2mA$$
$$= -1mA.$$

As $x < 0 \Rightarrow D_1 = OFF$. (Assumption fail).

D_1-OFF D_2-ON



$$I_2 = \frac{10+10}{15K}$$

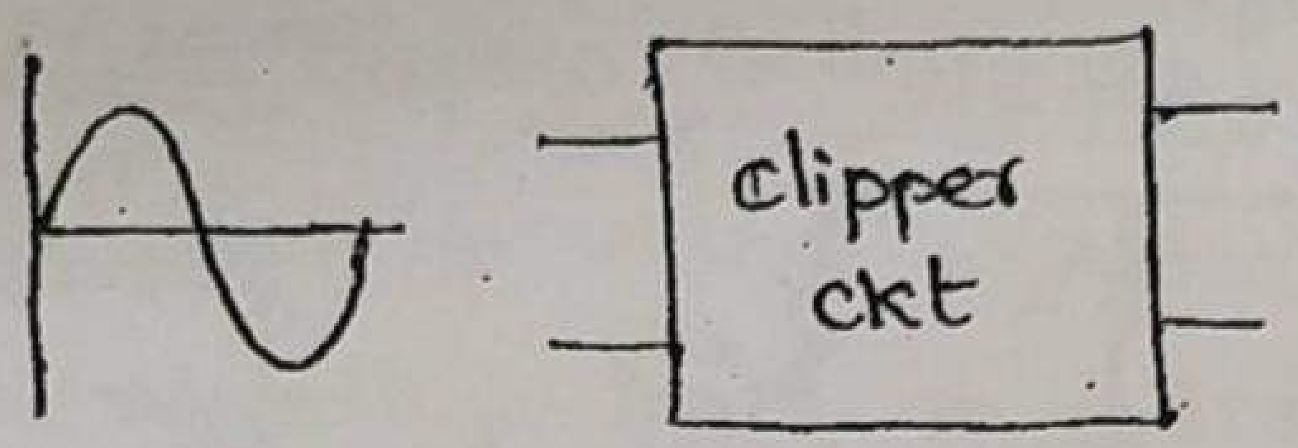
$$I_2 = 1.33A.$$

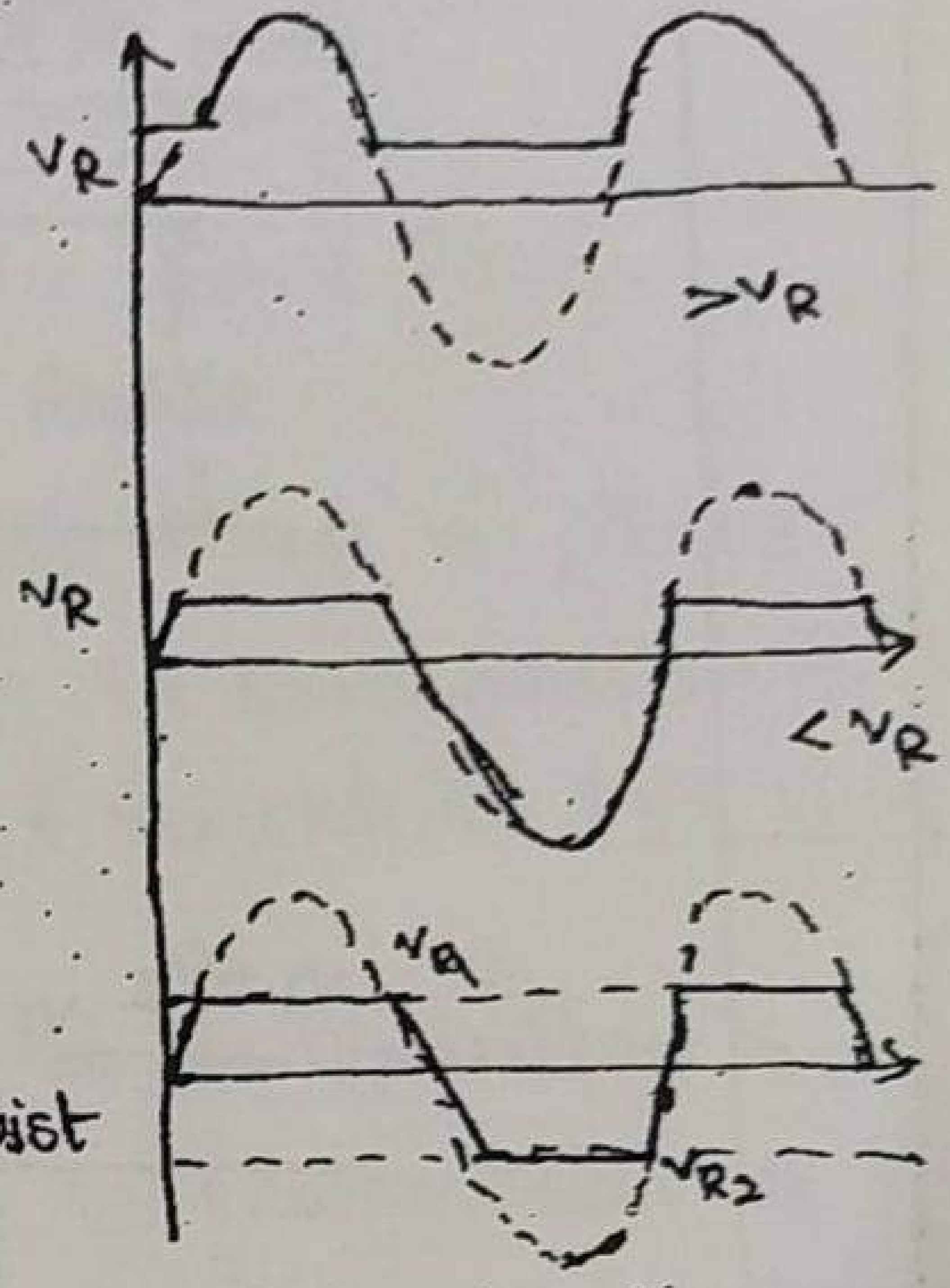
$$I_1 = 0A.$$

Applications of Diodes:-

1. CLIPPERS:-

* Clipper is a transmission ckt which transmits the i/p signal to the o/p either above the reference voltage (or) below the reference voltage (or) b/w the two reference voltages.





In b/w two V_R

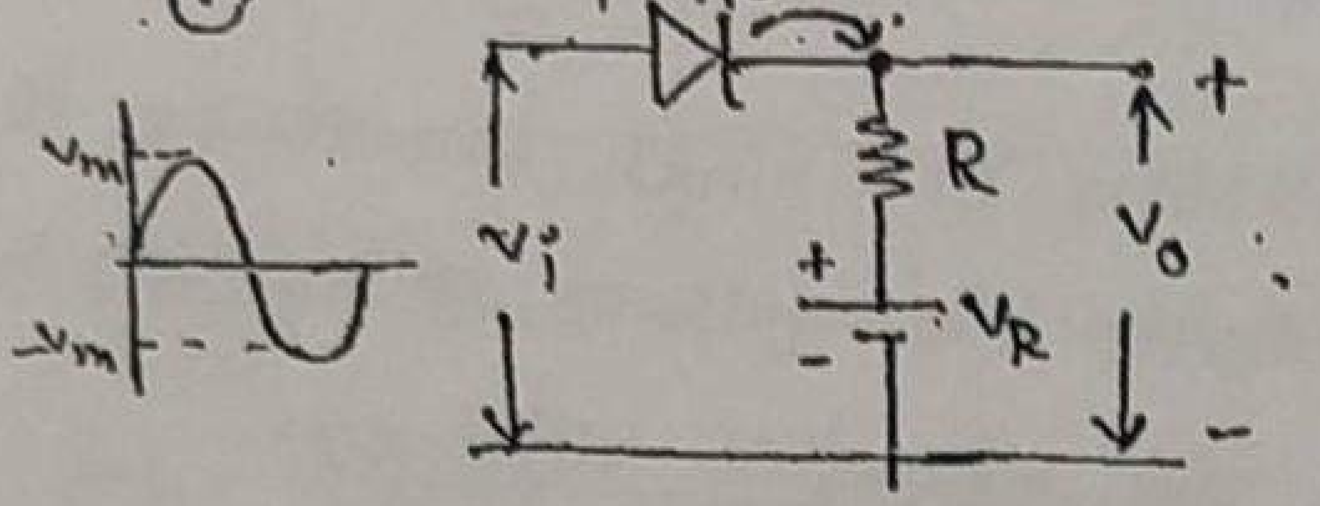
* clipper ckts are also called as "voltage selector ckts" (or) "voltage limiters".
* If the o/p of the clipper doesn't consist of +ve peak → <u>positive clipper ckt</u>
* If the o/p of the clipper doesn't consist of −ve peak → <u>Negative clipper ckt.</u>
* If the o/p of the clipper doesn't consist of both +ve & −ve peak → <u>SLICER ckt</u>

⇒ Clippers are classified into
- Single level clippers.
  - series clippers
    * In this i/p is given to diode
  - Shunt clippers
    * In this, o/p taken ~~acc~~ across the Diode branch
- Two level clippers [Slicer ckts]

→ clipper ckts doesn't consists of energy storage elements : L & C.
clipper ckt consist of → * Diodes, reference voltages, Resistors.

Series clippers:-

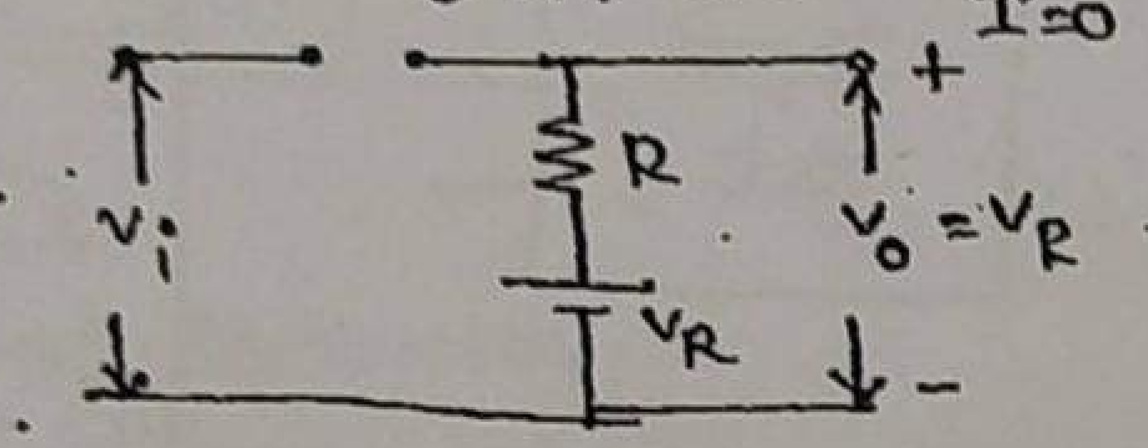
① P nD ⇒ ideal



$$V_0 = \begin{cases} V_i & \text{for } V_i > V_R \\ V_R & \text{for } V_i \le V_R \end{cases}$$

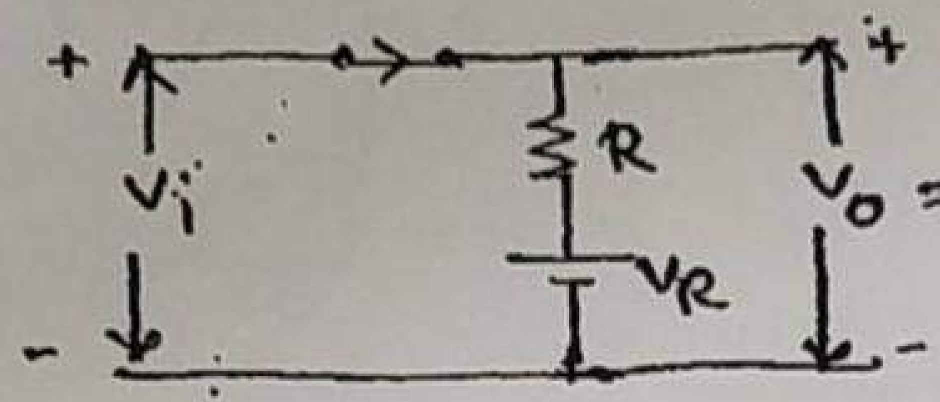
when $V_i \le V_R$:

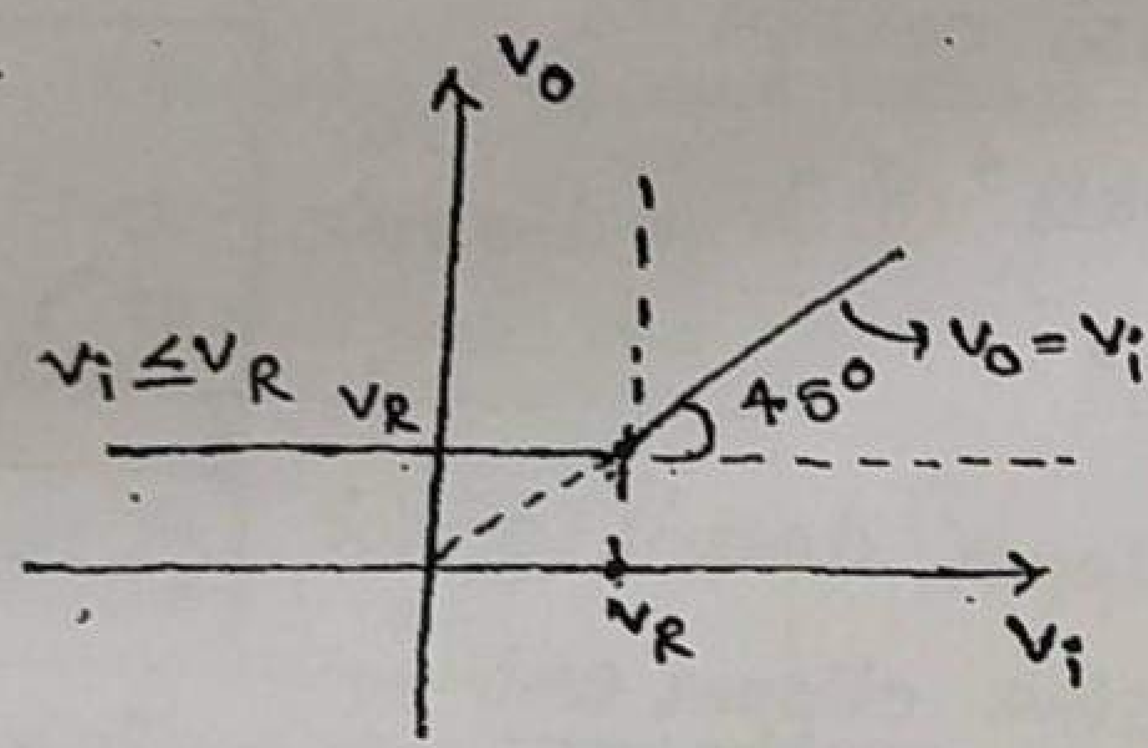
D-OFF-O.C

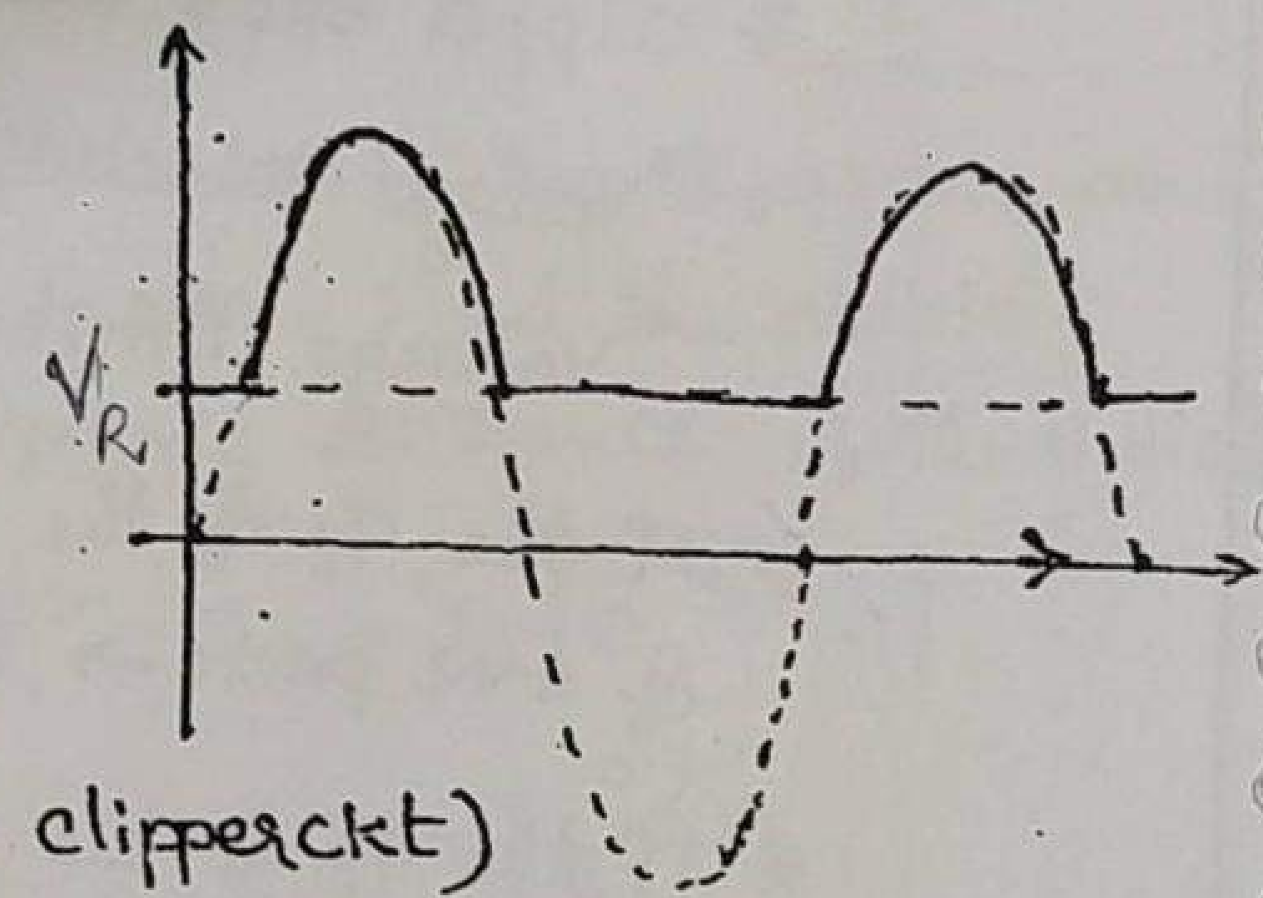


when $V_i > V_R$:-

D-ON → Replaced by s.c

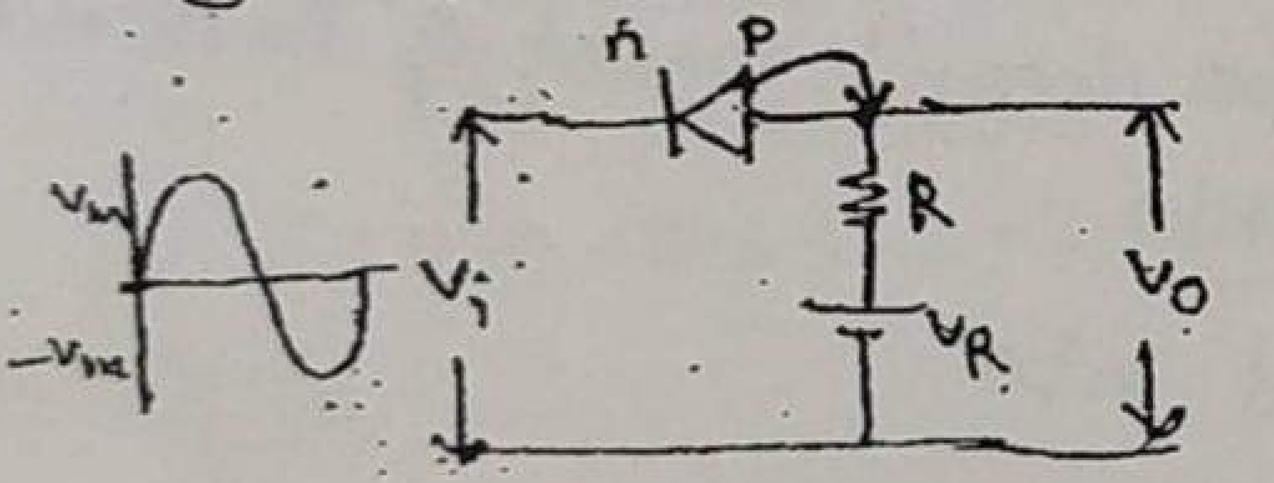






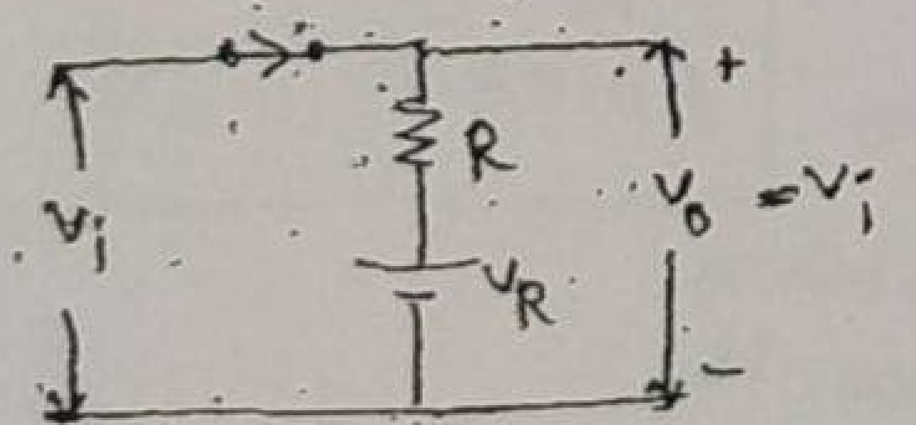
(Negative clipperckt)

② Reverse the diode so theckt is



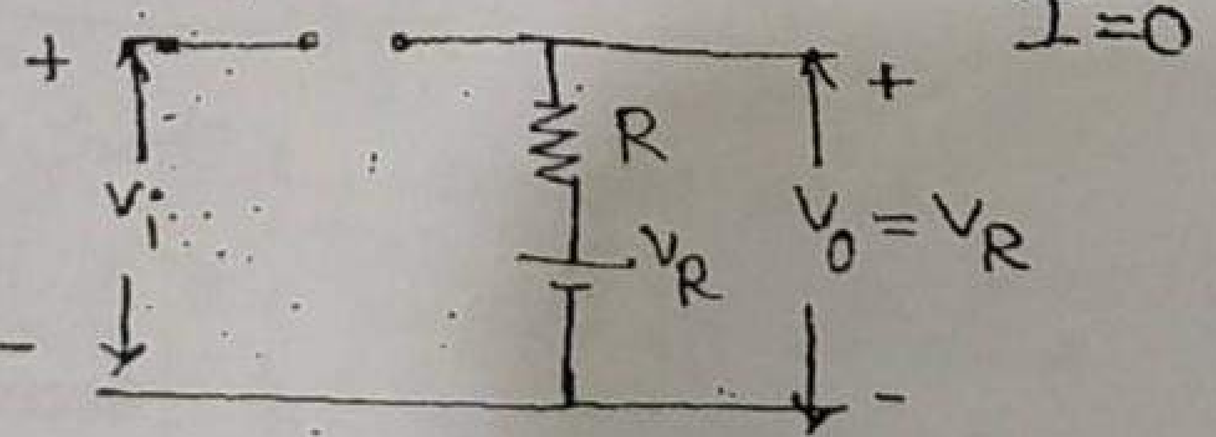
when $V_i < V_R$

D_1 - ON - replaced by s.c

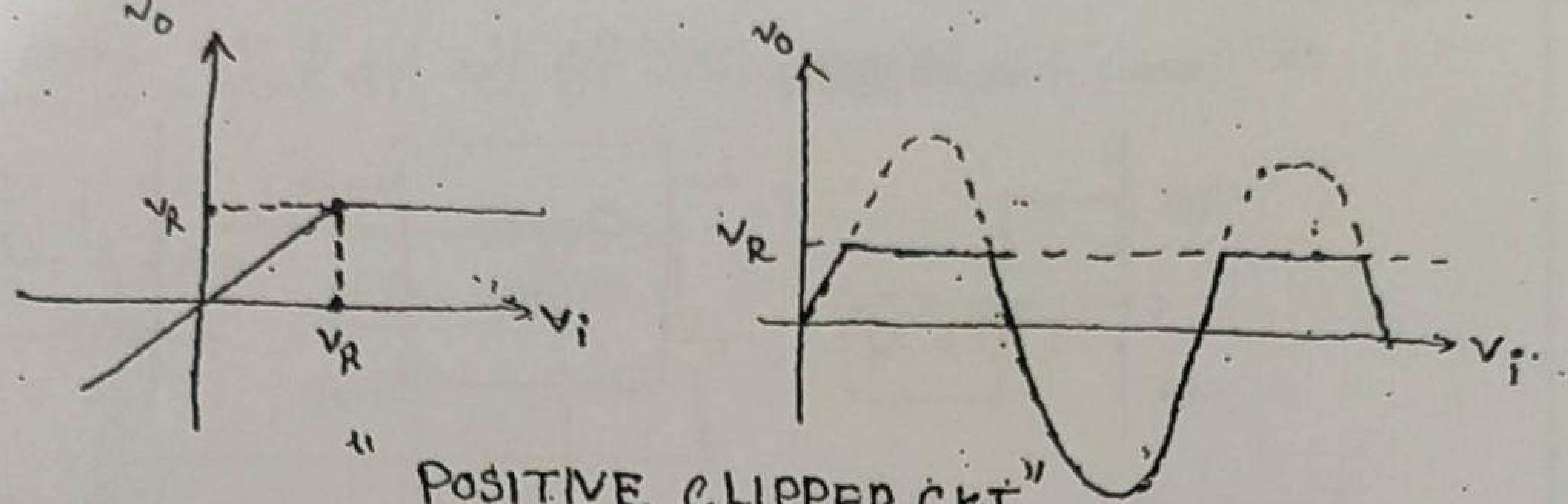


when $V_i \ge V_R$

D_1 - off - replaced by o.c



$$\boxed{\begin{aligned} V_0 &= V_i \text{ for } V_i < V_R \\ &= V_R \text{ for } V_i \ge V_R \end{aligned}}$$

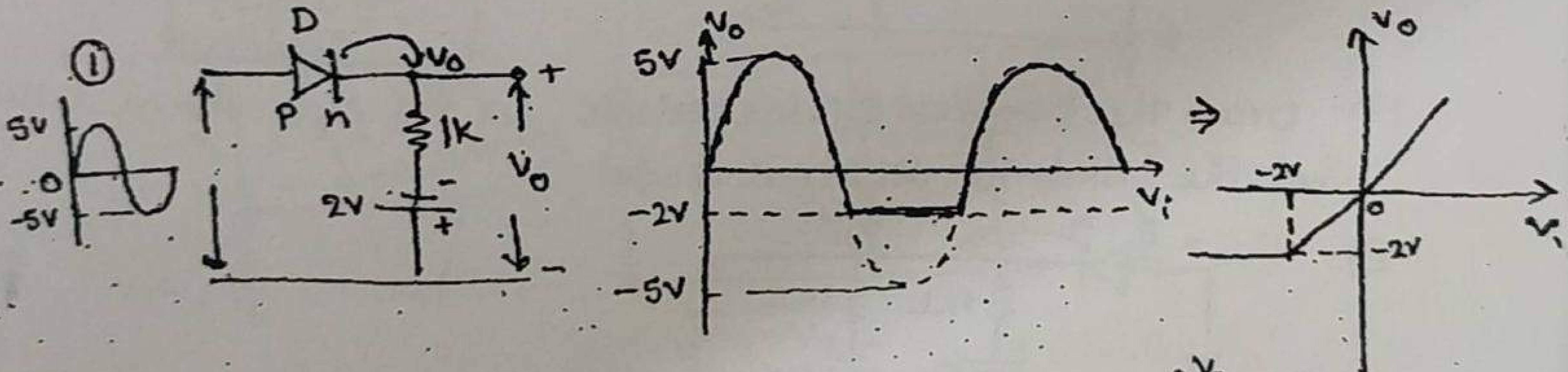


"POSITIVE CLIPPER CKT"

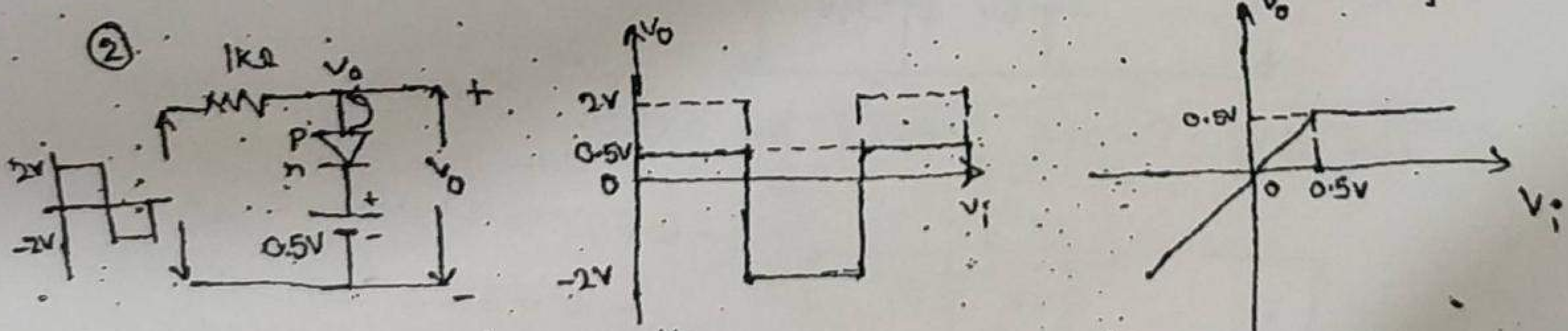
For single level clippers to draw o/p waveform:

1. Draw the given i/p voltage waveform in dotted form.
2. Draw the ref voltage levels in dotted format.
3. If P-type of diode connected to o/p voltage 'V_o', there should be no positive peak in the o/p i.e transmission of signal below the reference voltage & the ckt is +ve clipper ckt.
4. If N-type of the diode connected to the o/p voltage 'V_o', there should be no -ve peak in the o/p i.e transmission of signal above the ref voltage and the ckt is Negative clipper ckt.

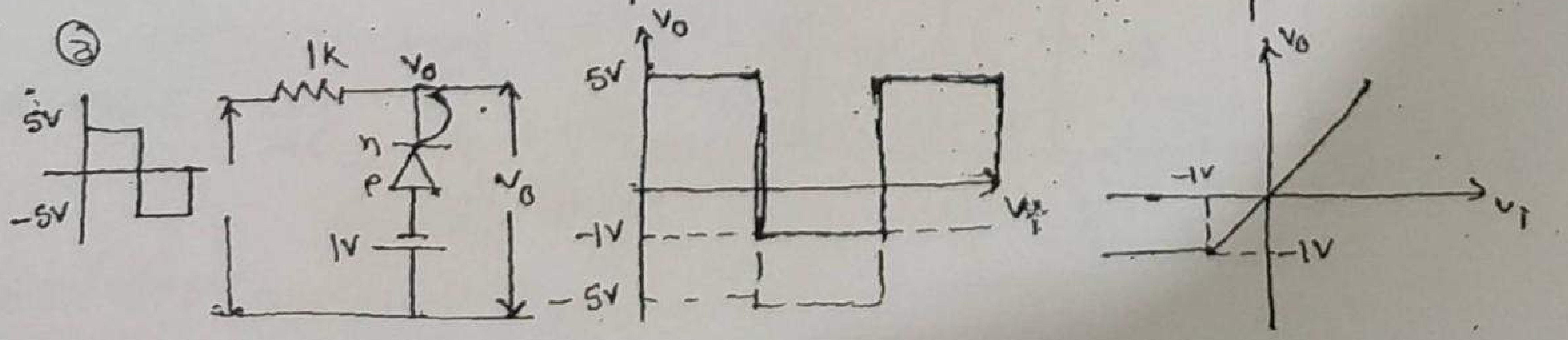
①



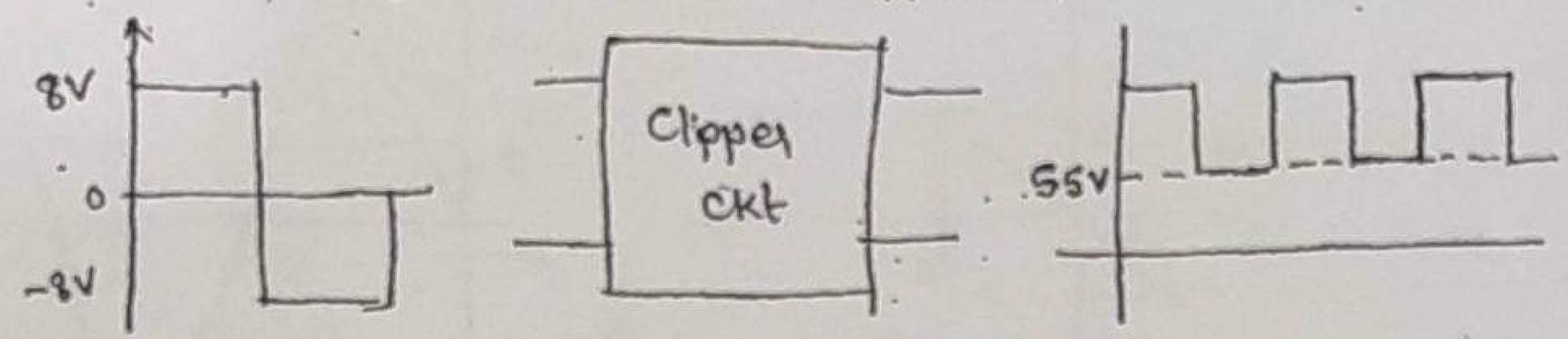
②



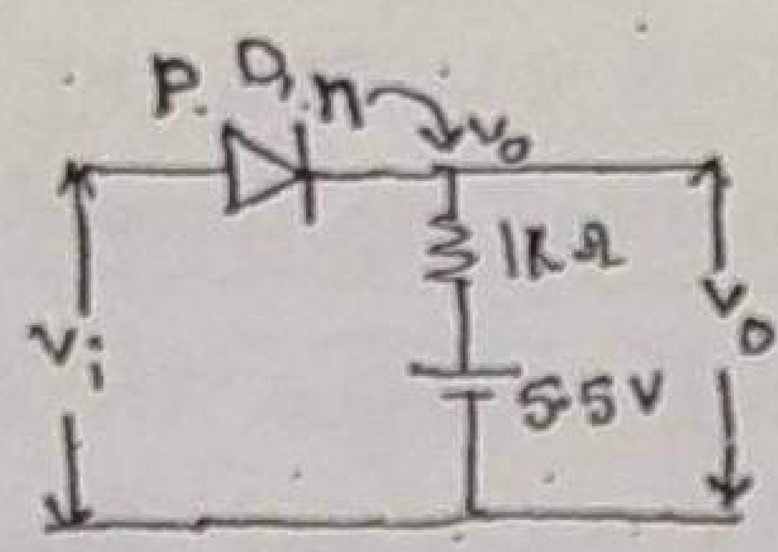
③



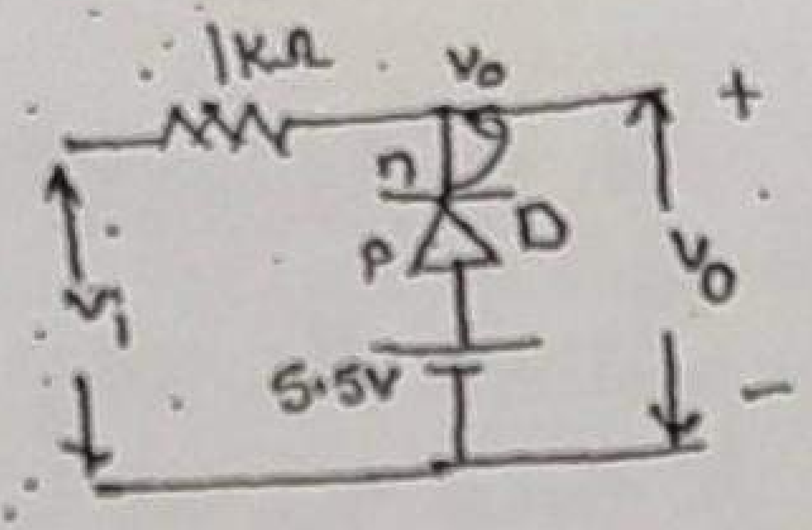
Pb:- Draw the clipper ckt for the i/p & o/p wavee form shown?



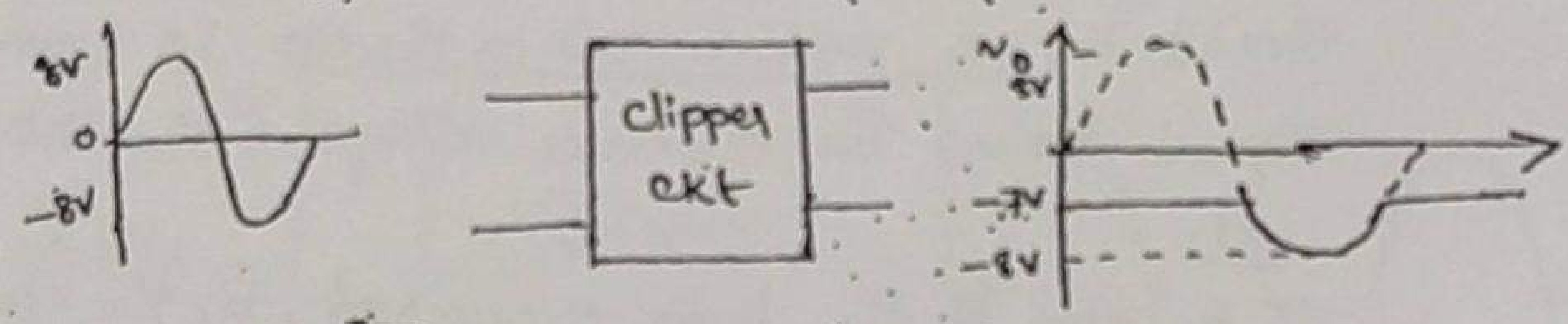
Sol:-



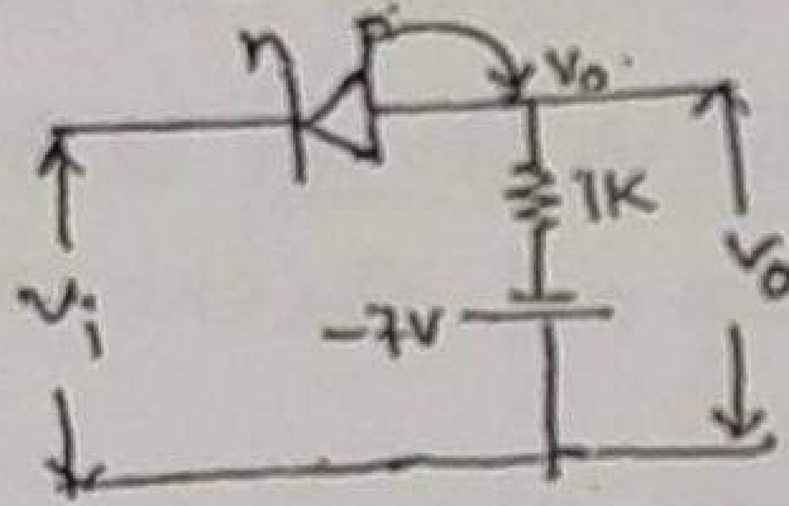
(or)



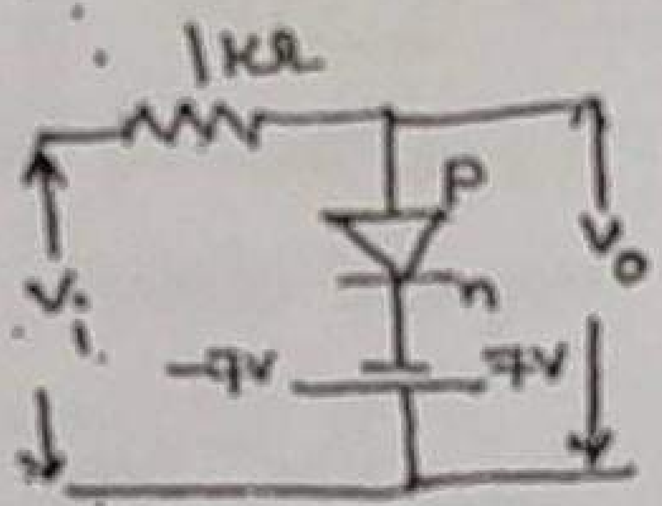
Pb:- Draw the clipper ckt for the i/p & o/p waveform shown?



Sol:-

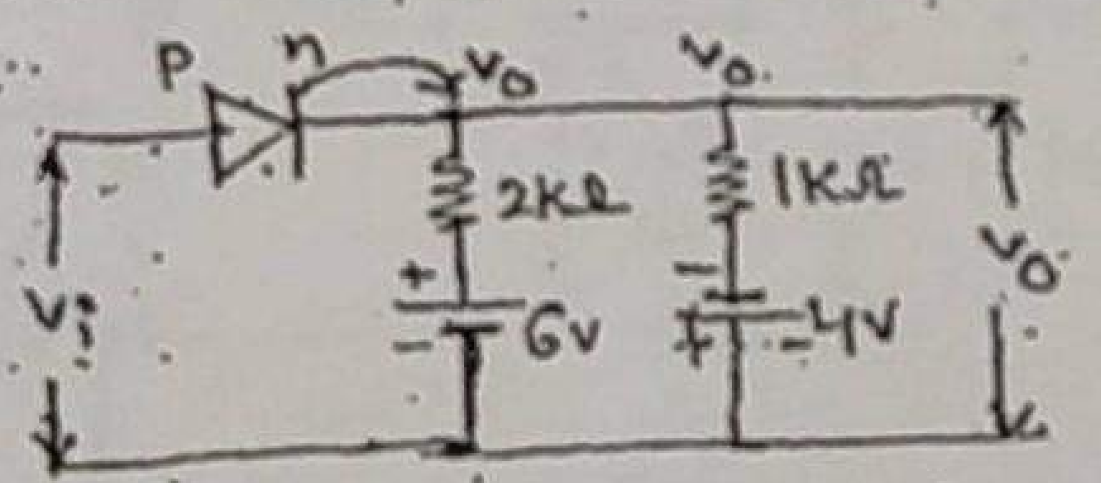


(or)

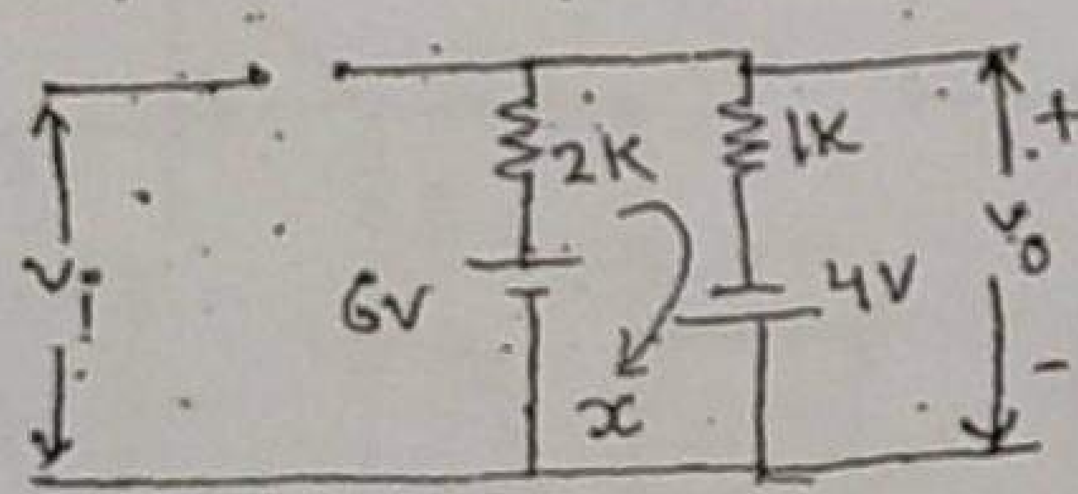


pb:- Draw the transfer characteristic for the ckt shown assume that the diode is an ideal diode.

Sol.-



$V_i \leq V_o$ D-off replace by o.ckt.



$-6+2Kx+1Kx-4=0$

$-10+3Kx=0$

$3Kx=10$

$x=\frac{10}{3K}=3.33mA.$

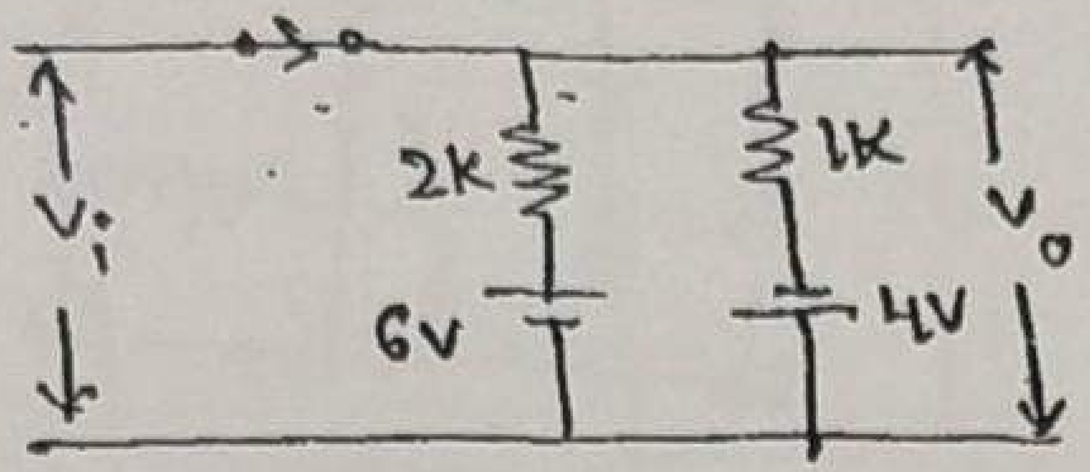
Now

$V_o-10^3x+4=0$

$V_o=-4+10^3x=-4+10^3\times 3.33m$

$=-4+3.33$

when $V_i > -0.67V$, D-ON → replaced by S.C

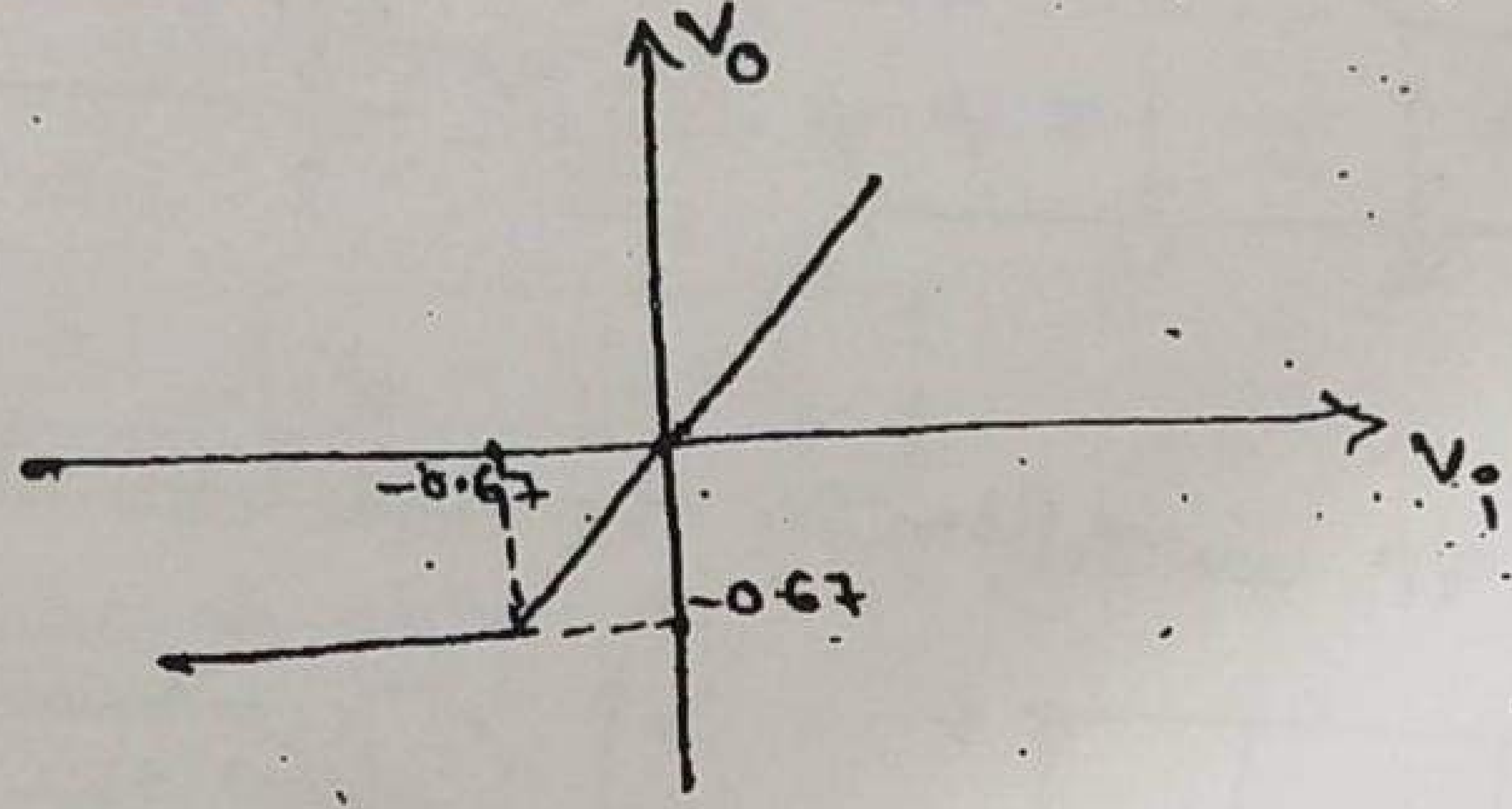


$\boxed{V_o = V_i}$

when $V_i \le -0.67V$ Doff → O.C $[V_o = -0.67V]$

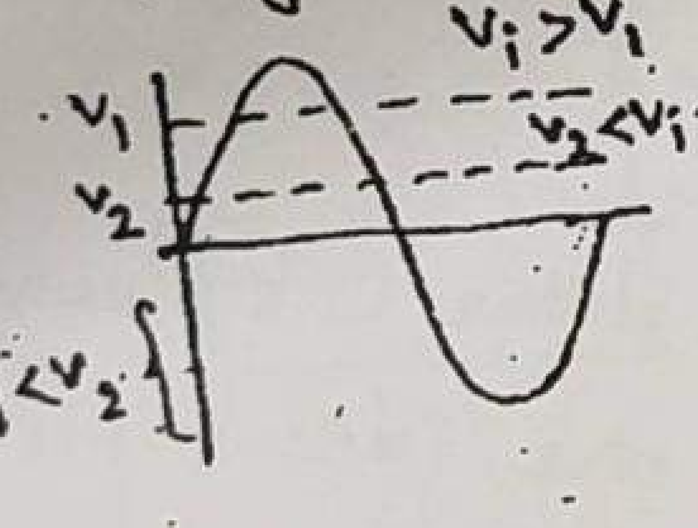
$V_i > -0.67V$ DON → S.C

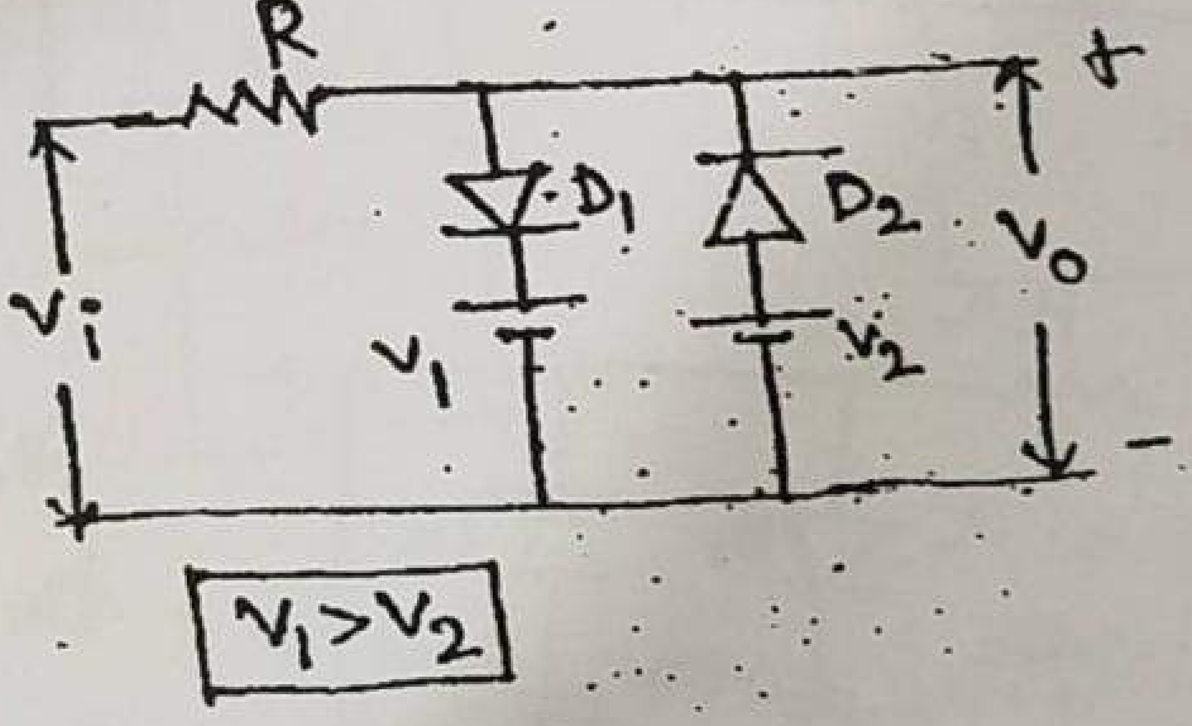
T/f characteristics:-



Two level clippers:-

This clipper ckt clips the signal at two independent Voltages



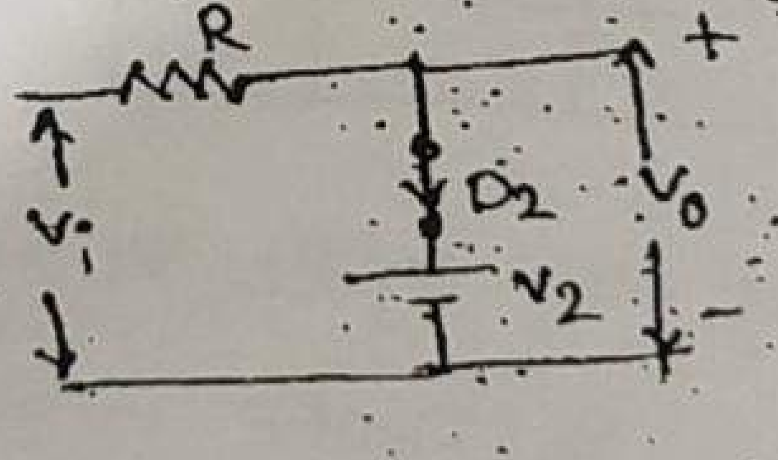


$\boxed{V_1 > V_2}$

case(i):- when $V_i < V_2$

D_1-OFF → O.C

D_2-ON → S.C

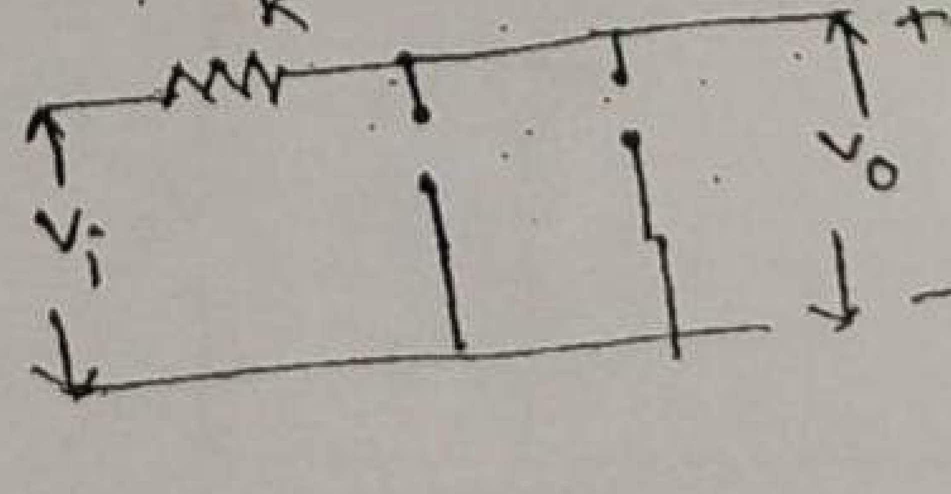


$\boxed{V_o = V_2}$

case(ii):- when $V_2 \le V_i < V_1$

D_2-off → O.C

D_1-OFF → O.C

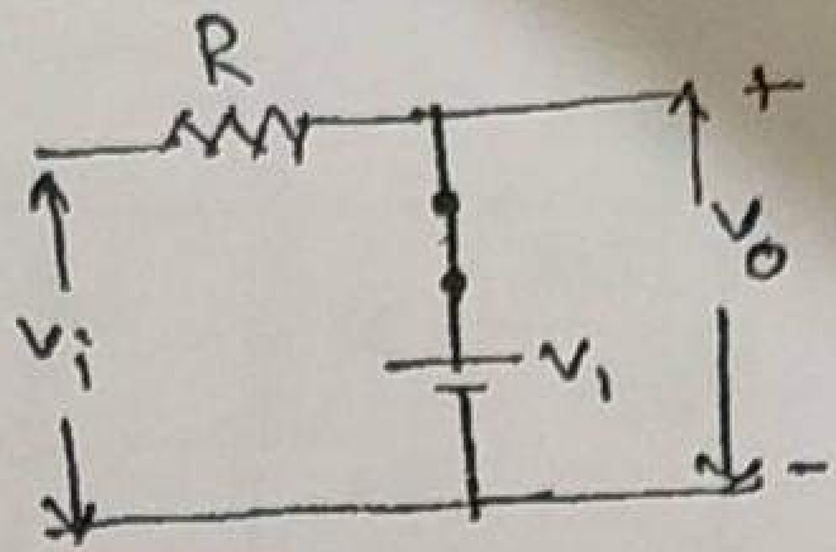


$\boxed{V_o = V_i}$

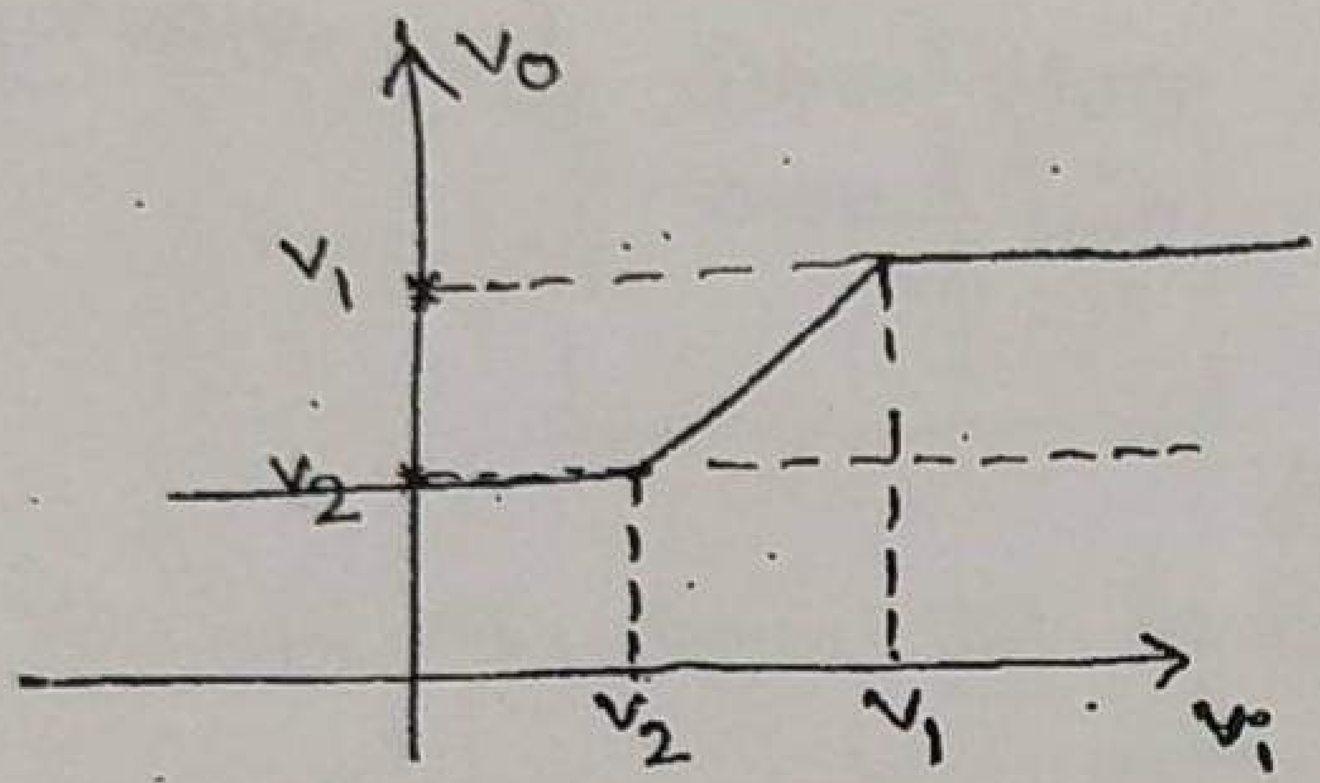
case(iii):- when $V_i > V_1$

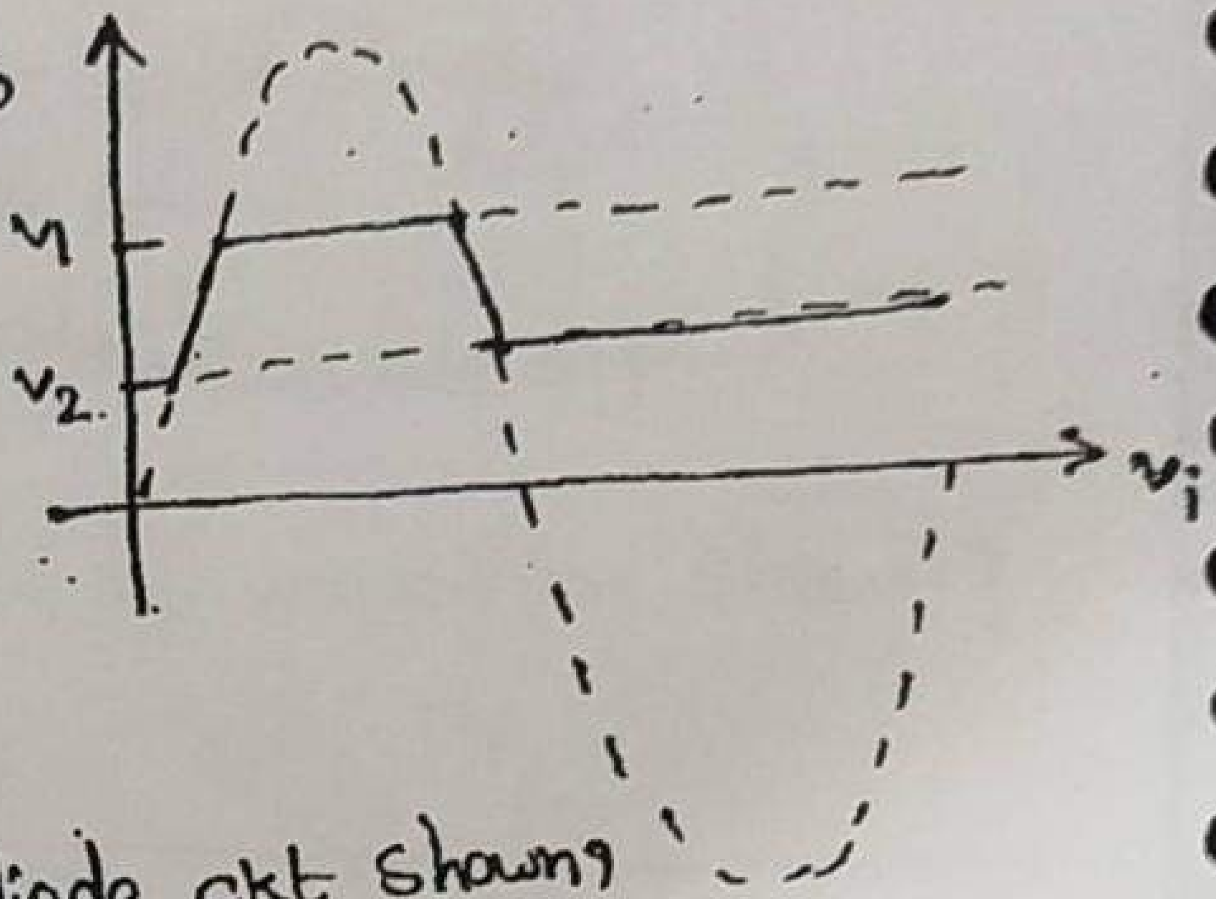
D_2 - OFF → O.C

D_1 - ON → S.C

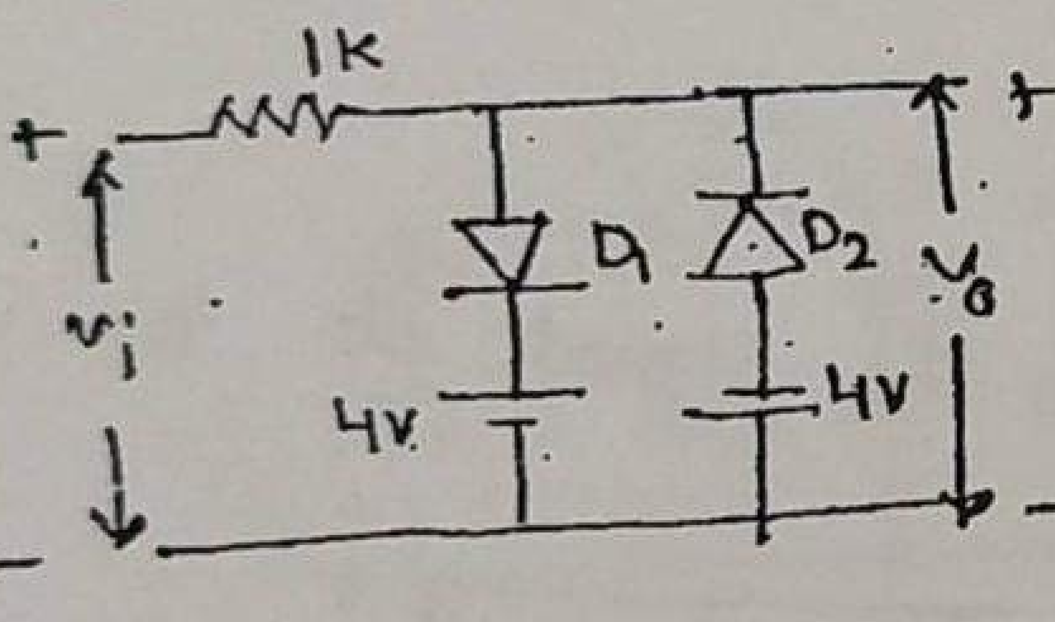


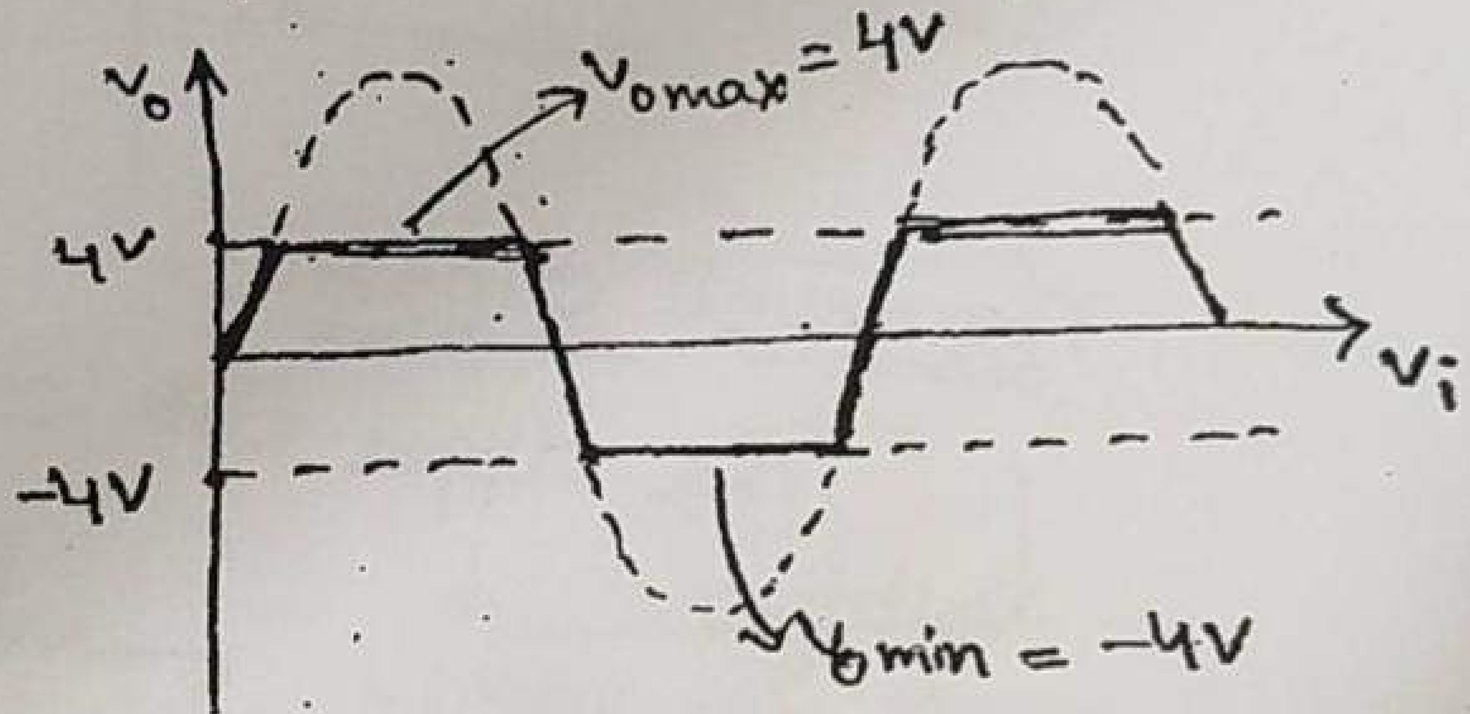
$\boxed{V_o = V_1}$



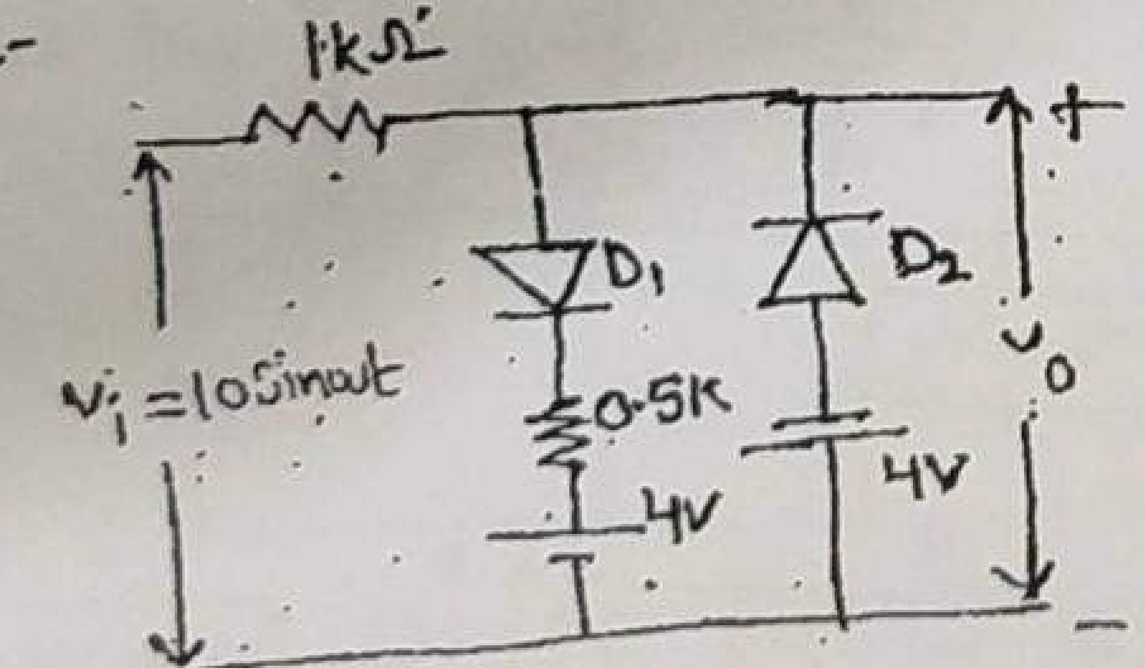


Pb:- Draw the o/p wave form for the diode ckt shown?





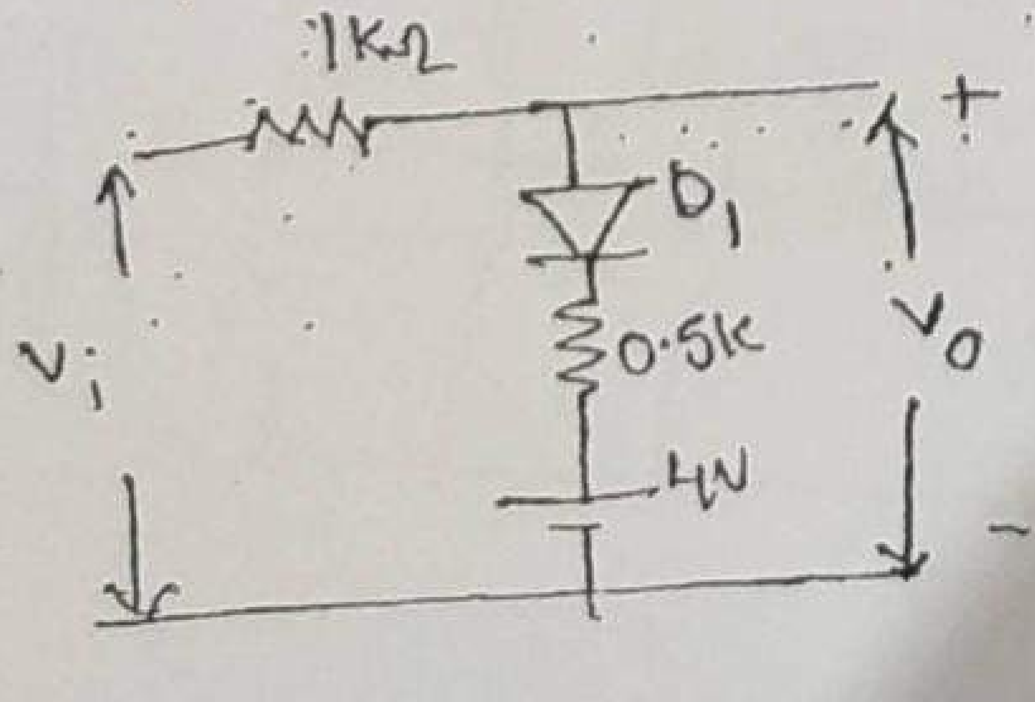
Pb:-



for the diode ckt shown, the diodes are ideal find the max & min values of o/p waveform.

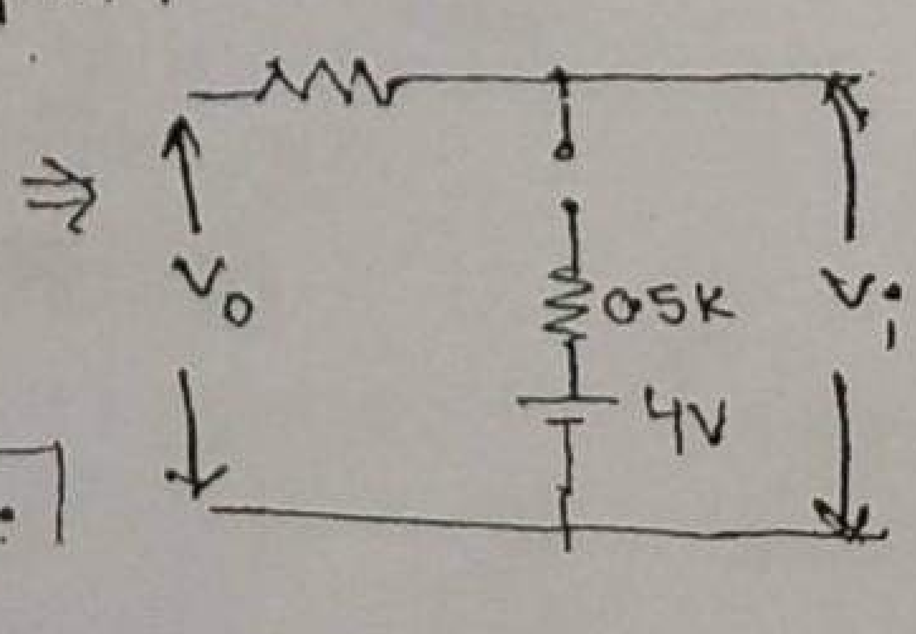
Sol:- During +ve cycle $V_i > 0V$

So D_2 OFF → O.C



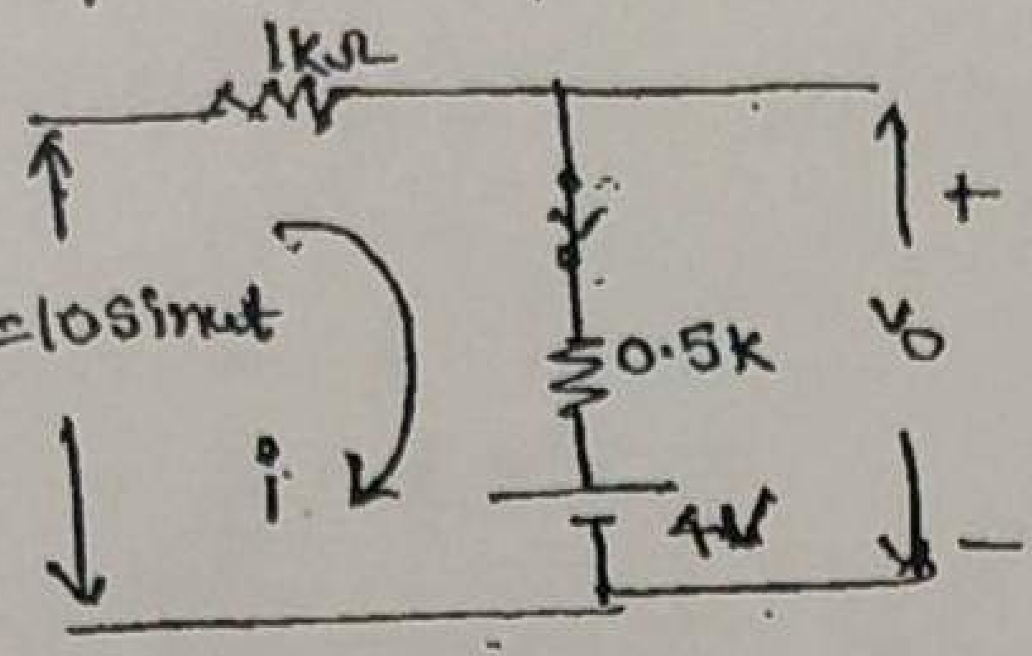
$V_i < 4$ D_1 - OFF

⇒



$V_o = V_i$

$V_i > 4V$ $\quad D_1 ON \longrightarrow S.C$



$$-V_i + 10^3 i + 0.5k\,i + 4 = 0$$

$$i(1.5\times10^3) - V_i + 4 = 0$$

$$i = \frac{V_i - 4}{1.5\times10^3}$$

$$V_o = 0.5\times10^3 i + 4$$

$$= 0.5\times\cancel{10^3}\times\frac{V_i-4}{1.5\times\cancel{10^3}} + 4$$

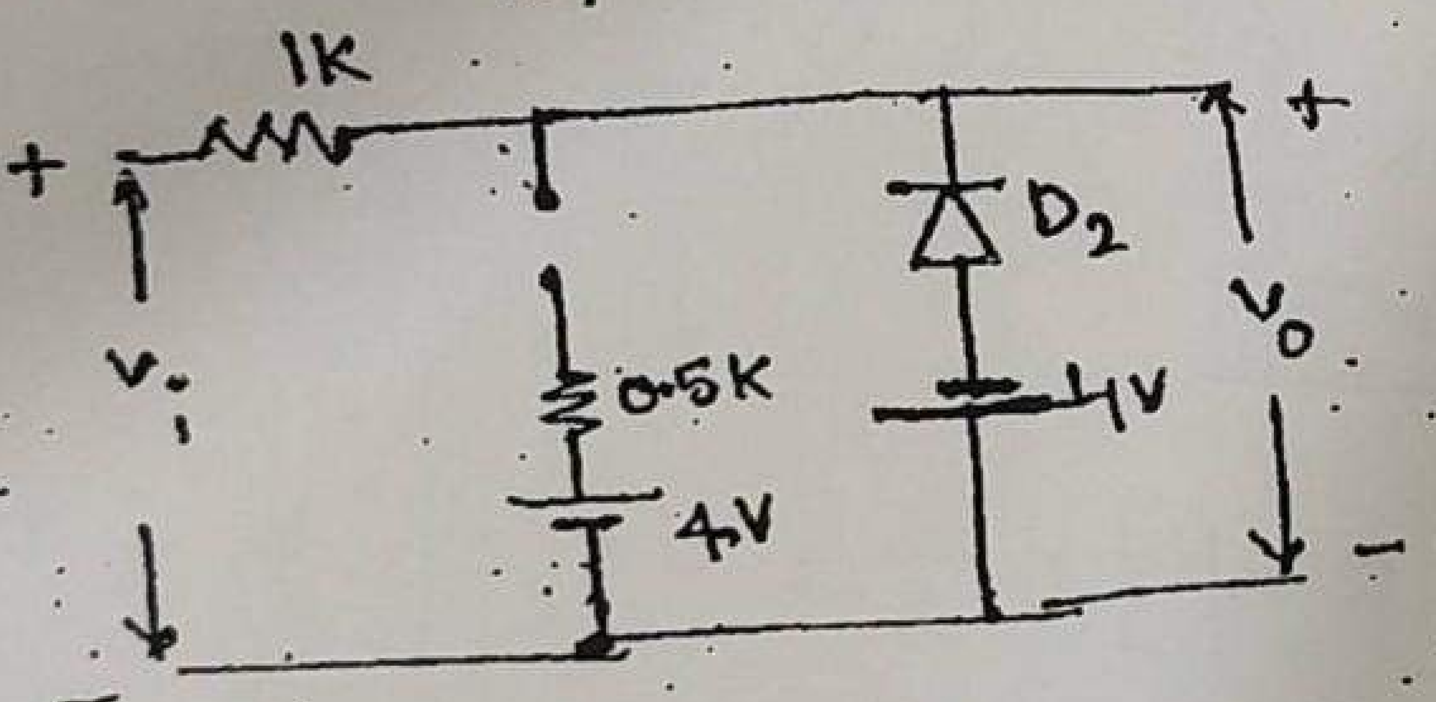
$$= \frac{V_i - 4}{3} + 4 = \frac{V_i}{3} - \frac{4}{3} + 4 = \frac{V_i}{3} + \frac{8}{3}$$

$$\boxed{V_o = \frac{V_i}{3} + \frac{8}{3}}$$

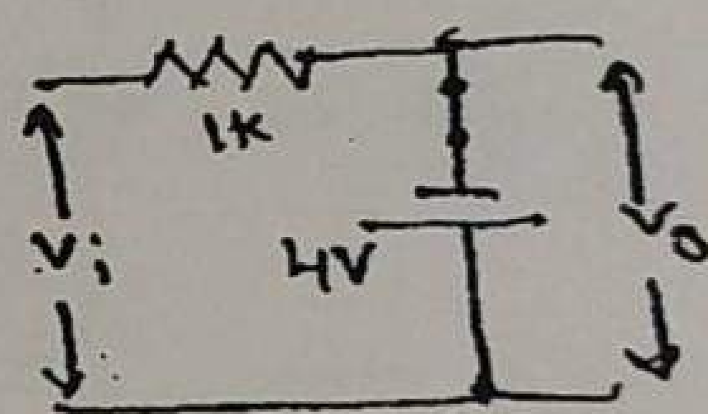
when $V_i = 10V$, $V_o = 6V$ (max)

During −ve cycle:-

D_1 OFF $\longrightarrow$ O.C

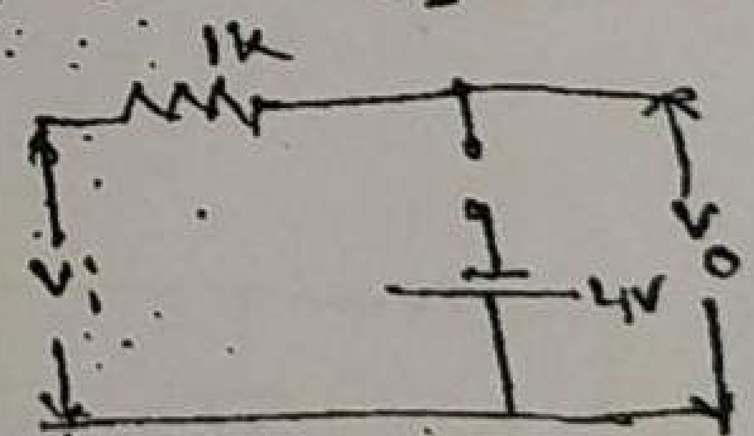


$V_i < -4 \Rightarrow D_2 ON \rightarrow S.C$

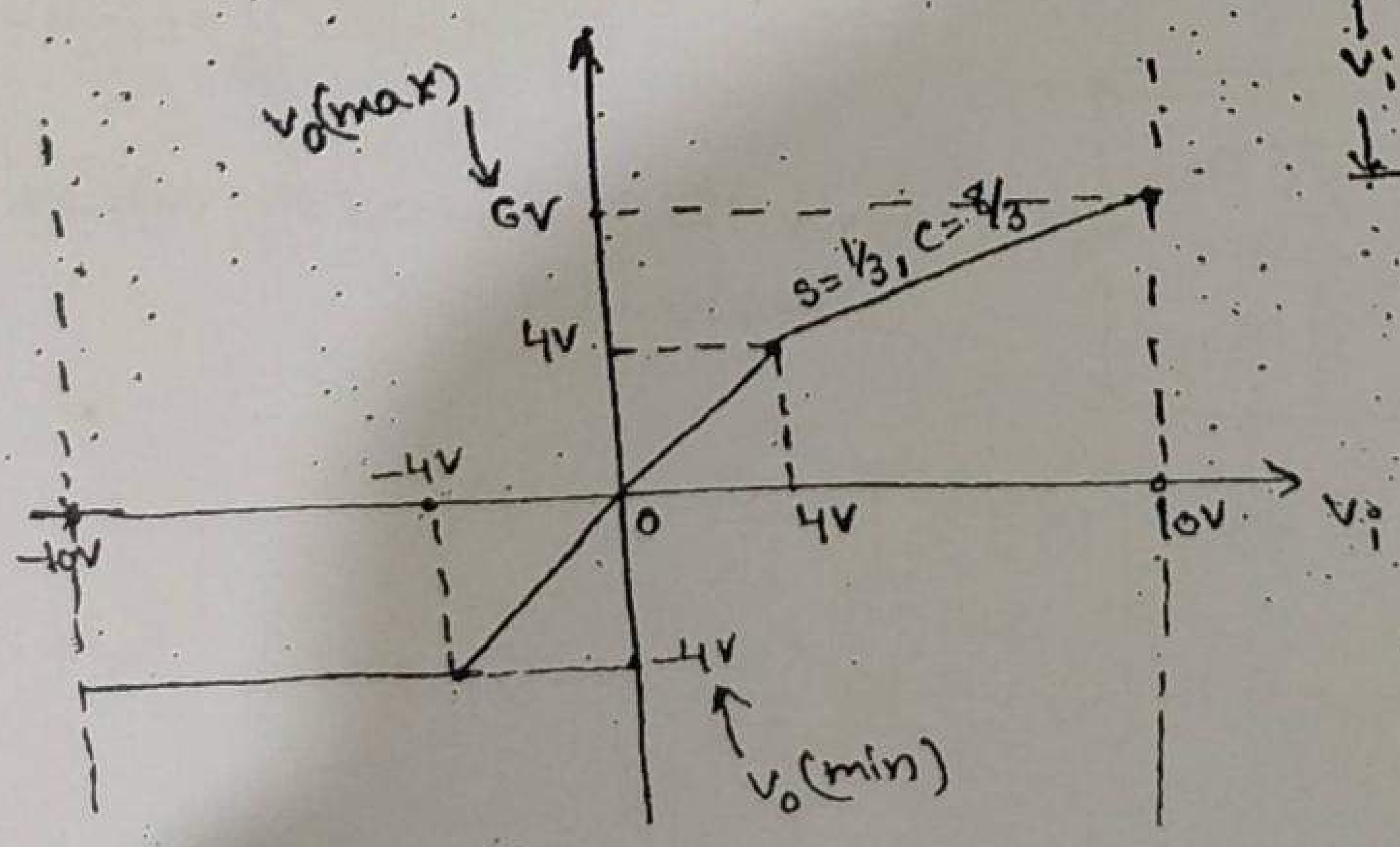


$$\boxed{V_o = -4V}$$

$V_i \geq -4 \Rightarrow D_2 OFF \rightarrow O.C$



$$\boxed{V_o = V_i}$$



CLAMPERS:-

→ The clamper ckts are used to shift the signal either upwards (or) downwards.

→ If the signal shifted upwards → clamper inserts +ve dc to the appiled signal → positive clamper ckt.

→ If the signal shifted downwards – clamper inserts –ve dc → Negative clamper ckt.

→ clamper ckts are also called as 'Dc inserter ckts' (or) 'Dc Restorer ckts'

→ All the restorer ckts are called inserters but not vice versa

→ clamper ckts consists of energy storage elements like 'C' or [L-Bulk, cost so L → not prefe

→ Input signal always given to capacitance only.

→ In clamper

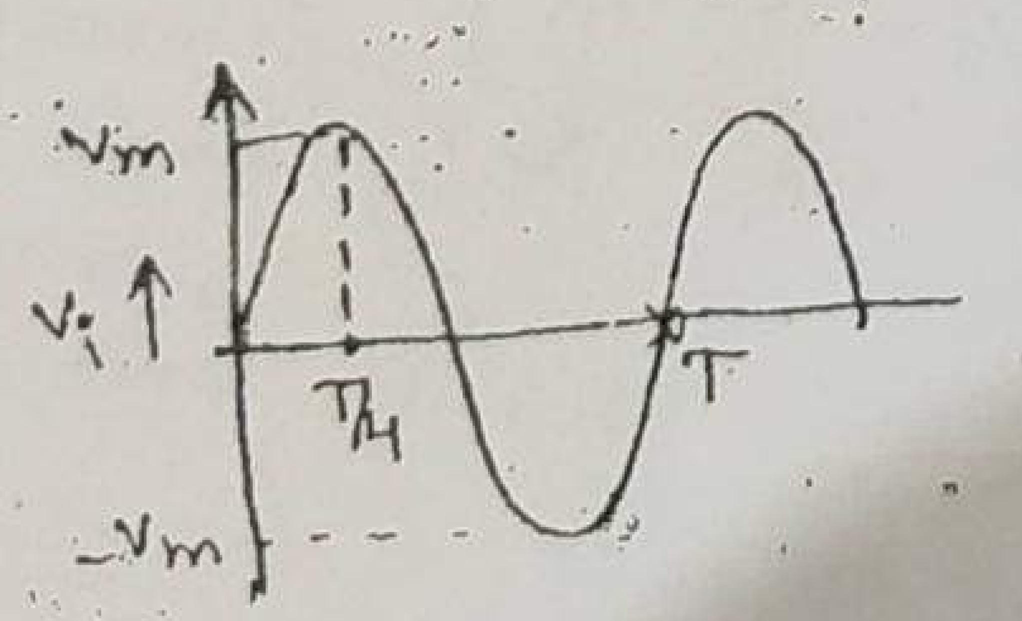
$$\boxed{(V_{p-p})_{o/p} = (V_{p-p})_{i/p}}$$

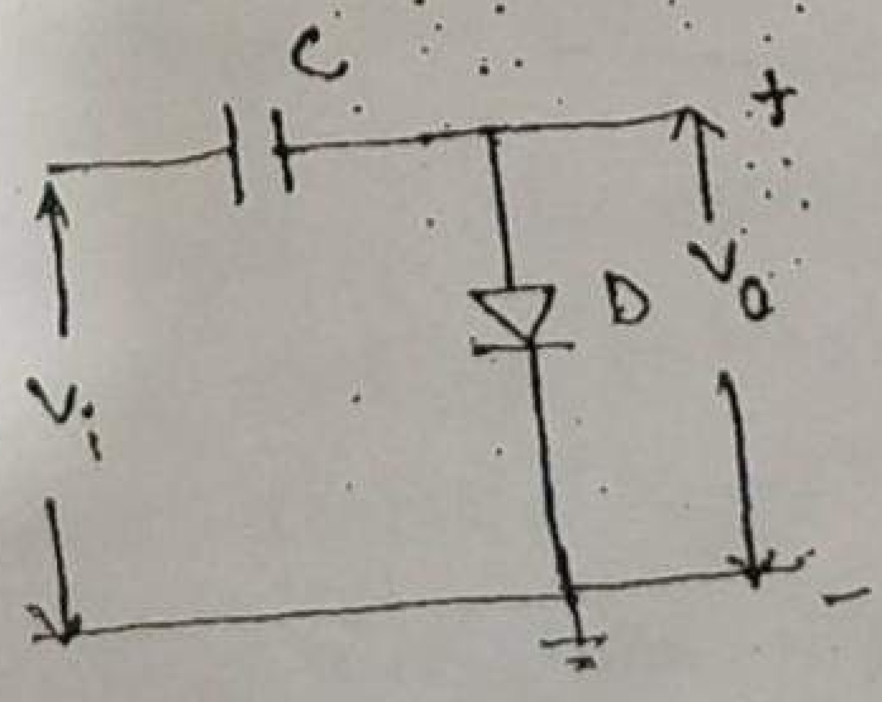
→ The analysis of a clamper ckt always starts with the conduction of diode.

clampers classified into 2 types
① Negative clamping.
② +ve clamping.

–ve clamping ckt also called as +ve peak clamper ckt
+ve clamping ckt also called as –ve peak clamper ckt

1. Negative clamping ckt:-

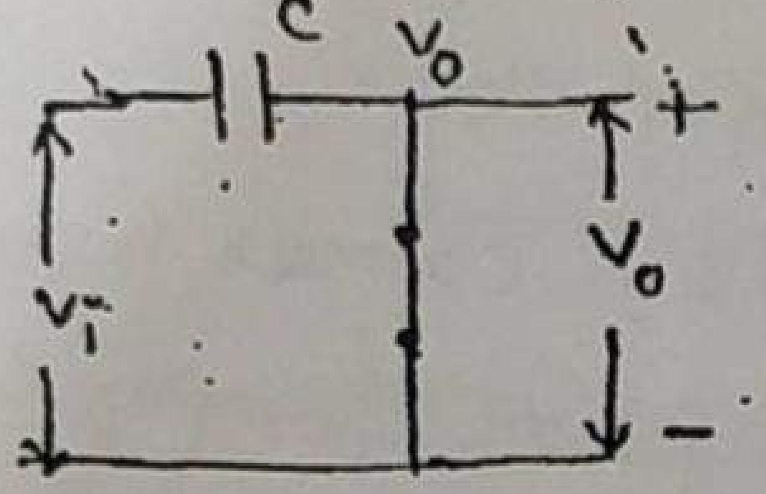




Let assume that the capacitor is initially uncharged

i.e $V_c = 0$ & diode is IDEAL $\begin{cases} \text{ON} & \text{S.C} \\ \text{OFF} & \text{O.C} \end{cases}$

when $V_i > 0$, D ON $\rightarrow$ S.C



$\boxed{V_0 = 0}$

$V_i - V_c - \cancel{V_0}^{0} = 0$

$V_i - V_c = 0$

$\boxed{V_i = V_c}$

The capacitor charges in accordance with the i/p voltage

when $t = T/4$; $V_i = V_m$

$V_c = V_m$ (the capacitor charges to the max value of V_m).

as $t = \frac{T}{4}^{++}$; $\boxed{V_c = V_m}$

$V_i < V_m$ (Just less than V_m)

$V_i - V_c - V_0 = 0$

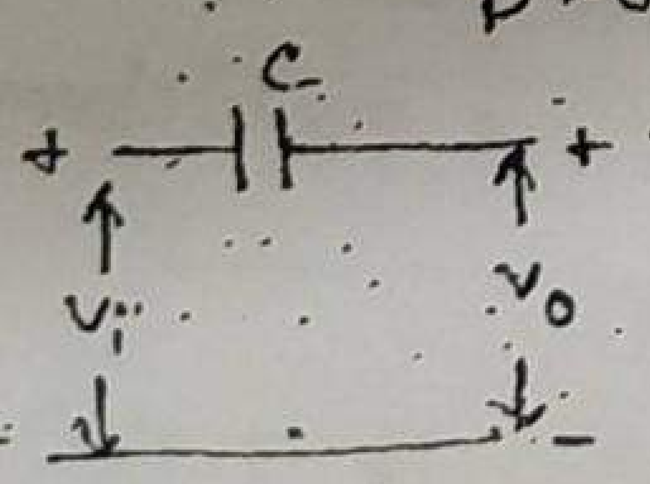
$V_0 = V_i - V_c$

$= \underbrace{< V_m - V_m}$

$\boxed{V_0 = -\text{ve voltage}}$

This negative voltage makes the diode off state

$\therefore$ D – off $\rightarrow$ replaced by o.c.



No discharge path for the capacitor so, capacitor holds the prev voltage

i.e $V_c = V_m$

$\boxed{V_0 = \underset{\text{A.C}}{V_i} - \underset{\text{D.C}}{V_m}}$

D.C inserted i.e clamper introduce $-V_m$ to applied V_i hence –ve clamper

At $t = T/4$, $v_i = V_m \Rightarrow \boxed{V_0 = 0}$

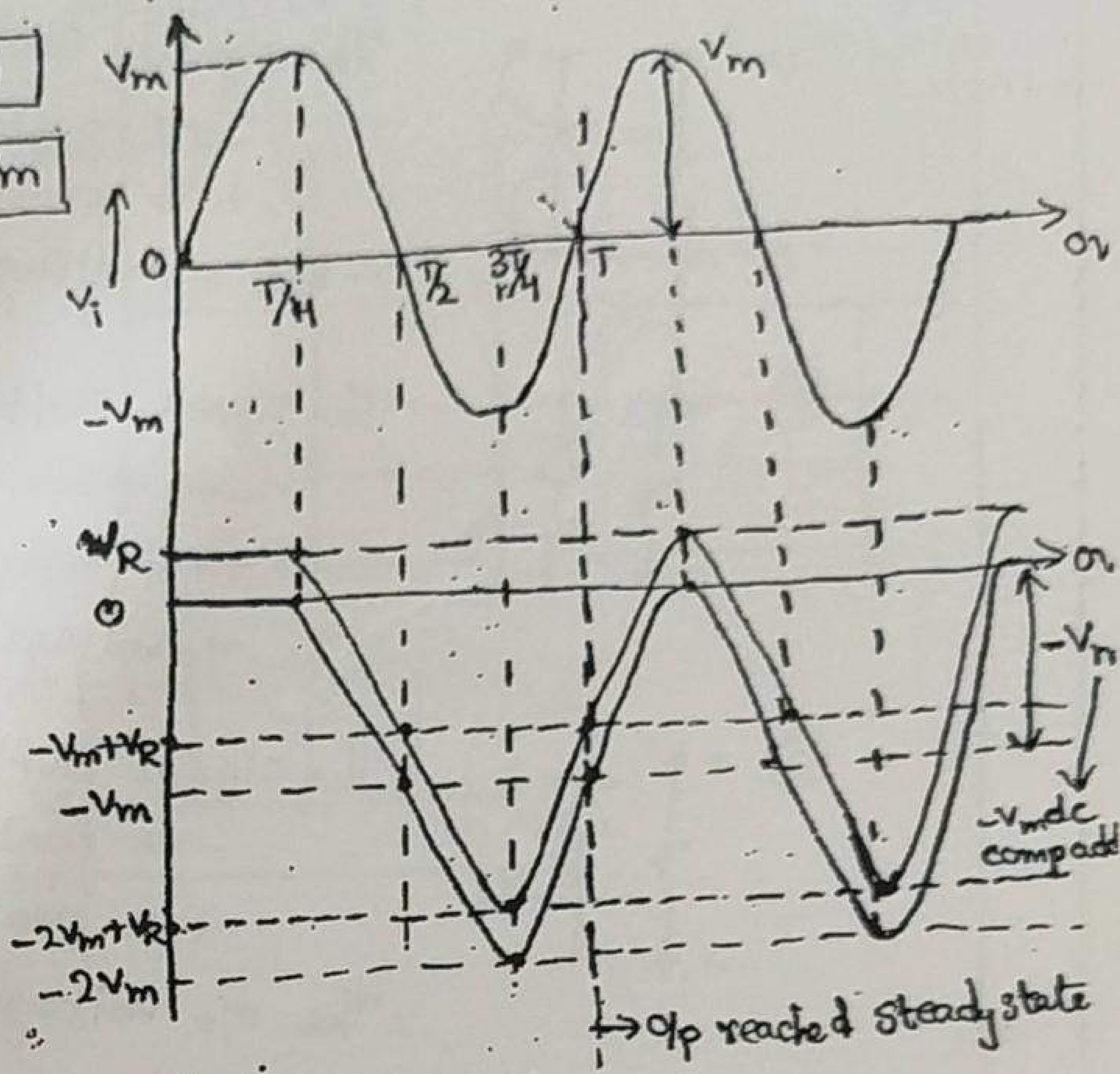
$t = T/2$, $v_i = 0 \Rightarrow \boxed{V_0 = -V_m}$

$t = \frac{3T}{4}$, $v_i = -V_m$

$\boxed{V_0 = -2V_m}$

$t = T$, $v_i = 0$

$\boxed{V_0 = -V_m}$

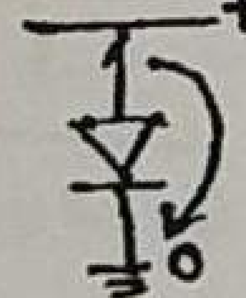


Hints:-

look the diode in ckt

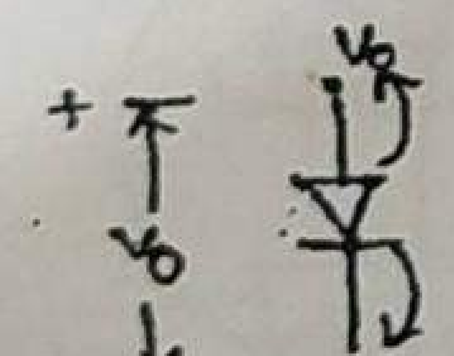
if the diode downwards, i/p is shifted downwards only.

what level shifted



(+ve peak shifted to 0).

①



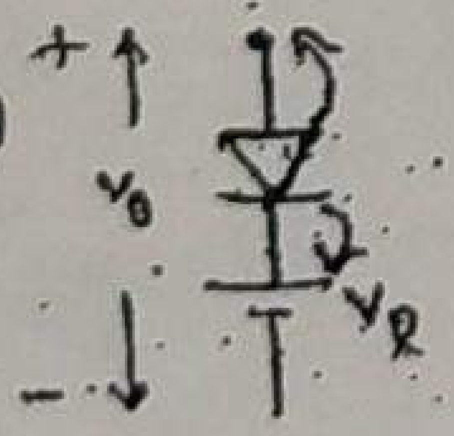
This shifts the signal downwards

+ve peak shifted to 0V

-ve peak shifted to $-2V_m$

$\therefore$ The o/p voltage levels are: 0 to $-2V_m$

②



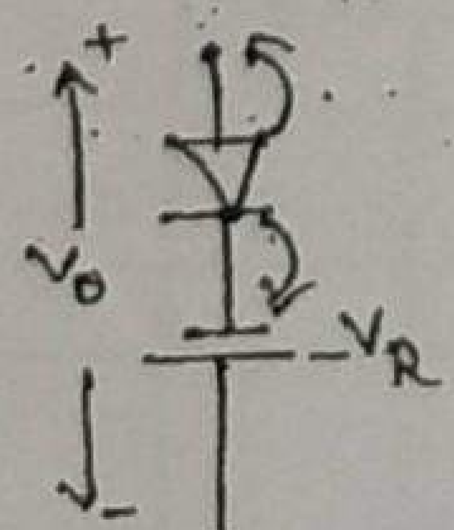
The signal shifted downwards

+ve peak shifted to V_R

-ve peak shifted to $-2V_m + V_R$

$\therefore$ The o/p voltage levels are: V_R to $-2V_m + V_R$.

③



The signal shifted downwards

+ve peak shifted to $-V_R$

-ve peak shifted to $-2V_m - V_R$

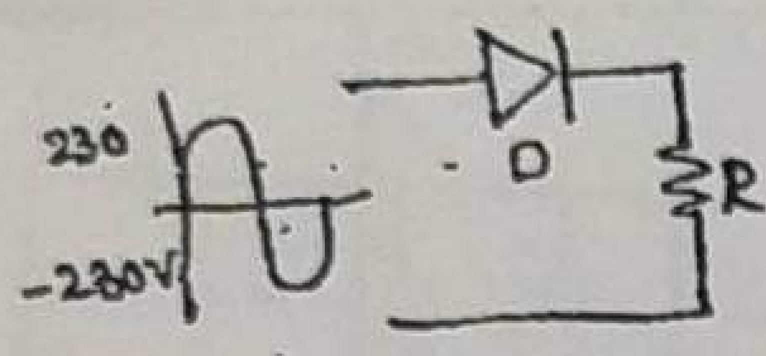
$\therefore$ The o/p voltage levels are $-V_R$ to $-2V_m - V_R$.

29/08/12

RECTIFIERS:-

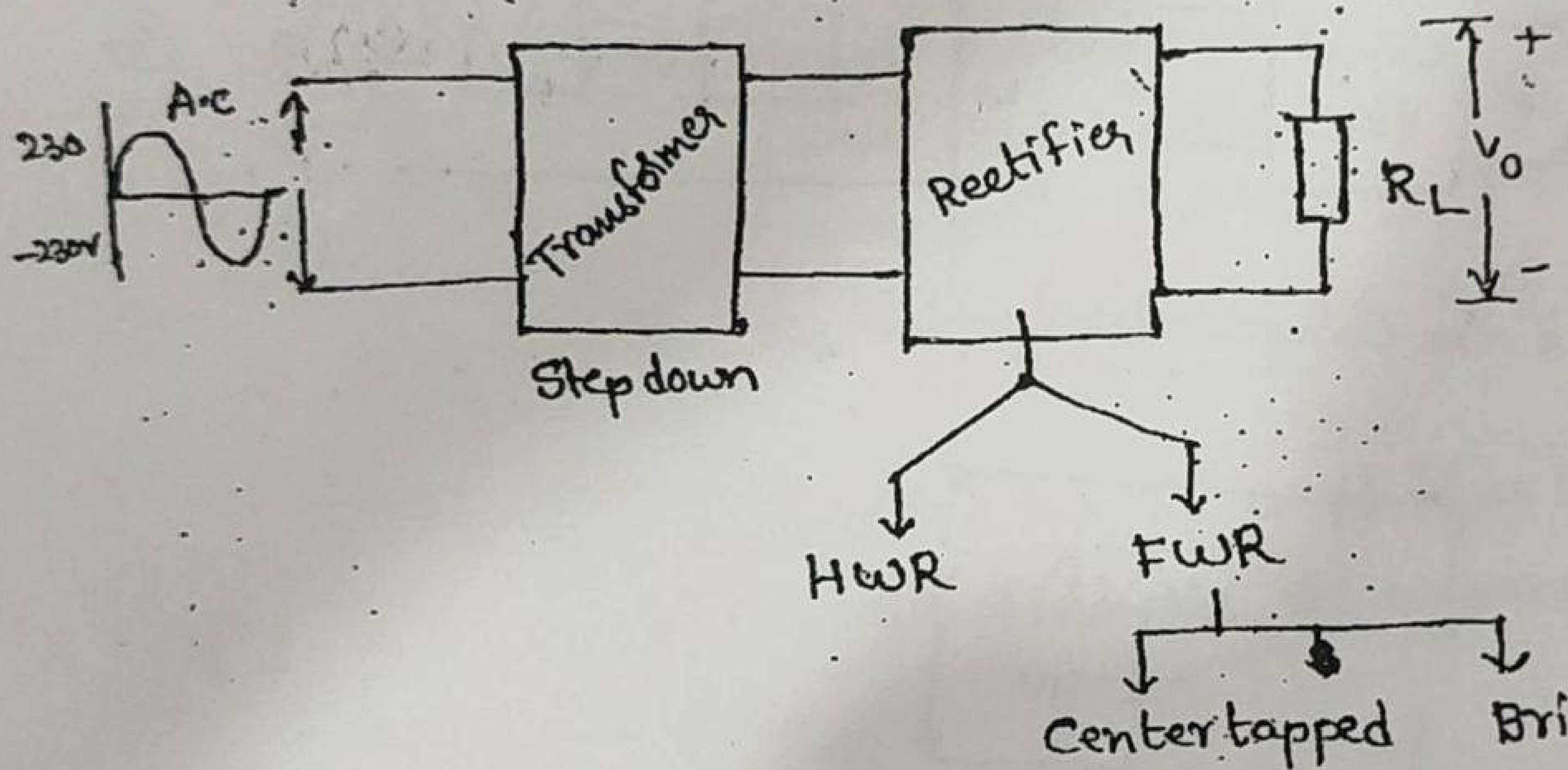
→ converts the AC signal into pulsating d.c

→ " Bidirectional signal into unidirectional signal.

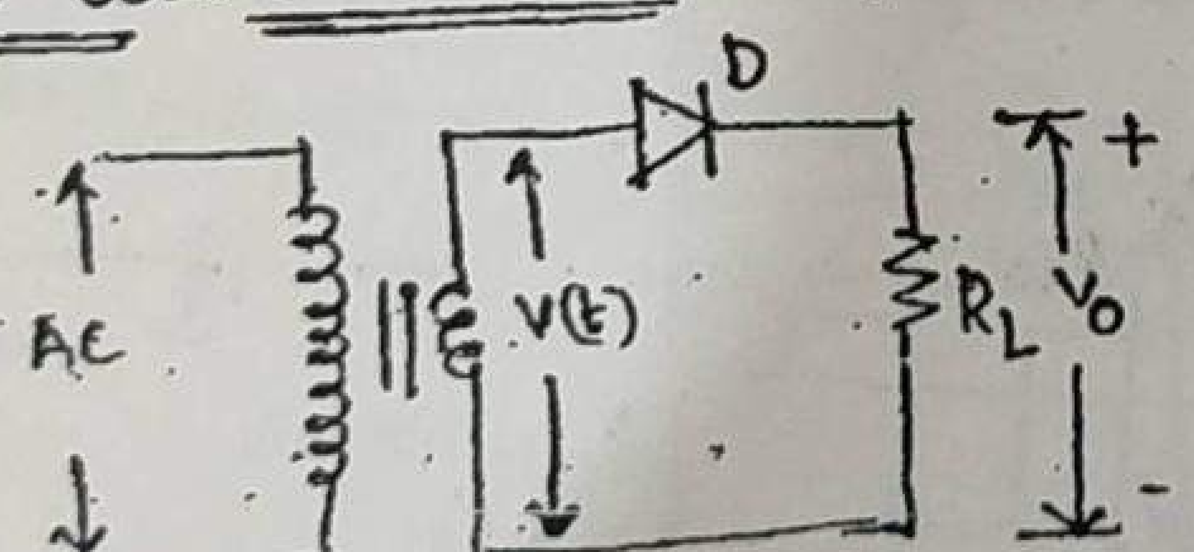


Diode cannot withstand with such high voltage. if such high vol is appiled permenant damage to diode occurs. Hence reduce the amplitude level is necessary, it is done by a stepdown t.F.

Block diagram of Rectifier:-



Half wave Rectifier:-



$v(t) = V_m \sin\omega t$

V_m = max value of the seconda

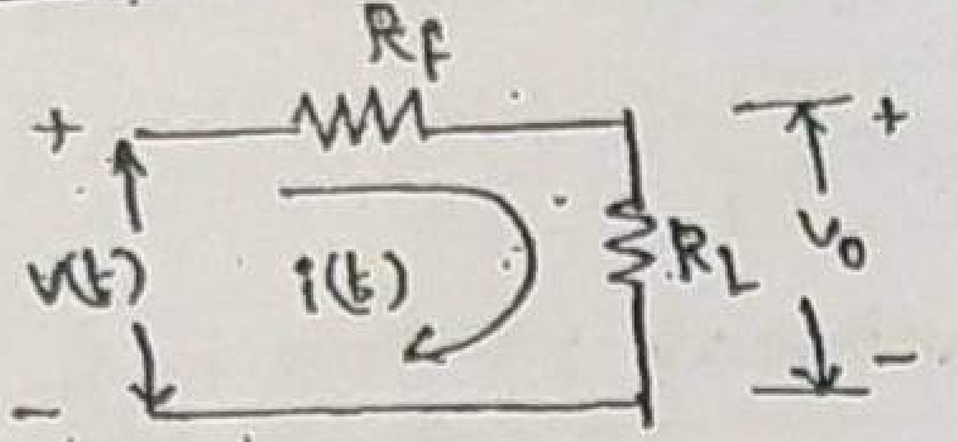
electronic T/F → 230 / 6(9) 12, 15 ... (3, 9) → [These values are not peak but rms values. (max = $6\sqrt{2}$, $9\sqrt{2}$ ...)]

Let $V_m >> V_\gamma$ → V_γ is neglected, and R_f of diodes is considered

when, D - F.B → Replaced by 'R_f'

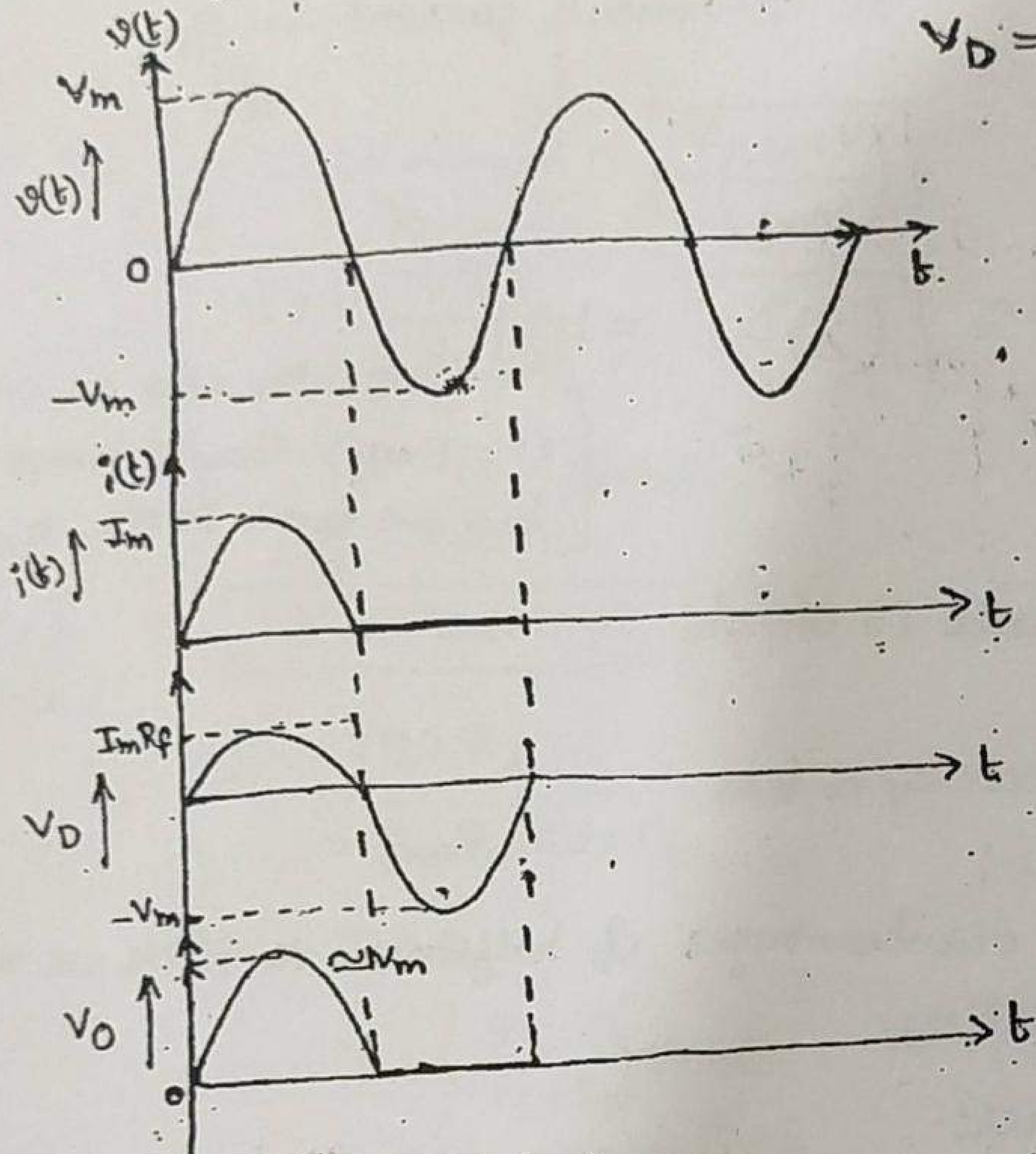
D - R.B → Replaced by 'O.C'.

During +ve cycle of $v(t)$:- D-ON-replaced by 'R_f'



$$i(t) = \frac{V(t)}{R_f + R_L} = \frac{V_m}{(R_f + R_L)} \sin\omega t$$

$$\boxed{i(t) = I_m \sin\omega t}$$



$$V_D = i(t) R_f = (I_m R_f) \sin\omega t$$

$$V_D = V_m \left(\frac{R_f}{R_f + R_L}\right) \sin\omega t$$

$R_f << R_L$ $\quad I_m R_f \to$ small

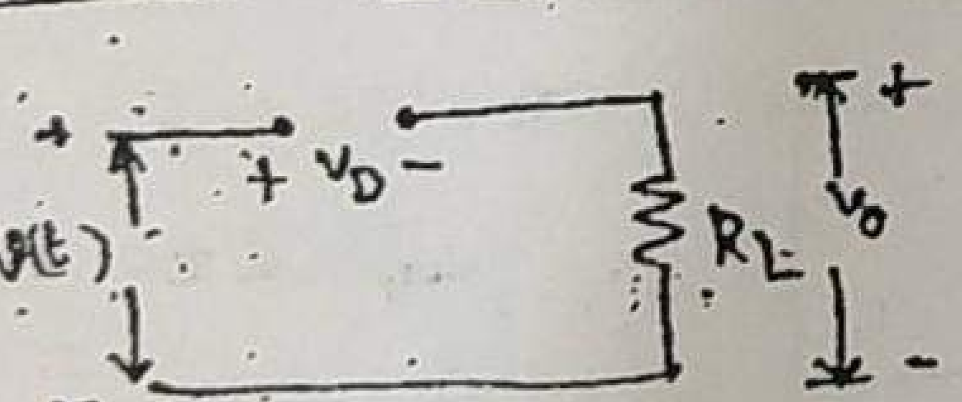
$$V_0 = i(t) R_L$$

$$= V_m \left(\frac{R_L}{R_L + R_f}\right) \sin\omega t$$

$R_L >> R_f$

$$\boxed{V_0 \simeq V_m \sin\omega t}$$

During -ve cycle of $v(t)$:- D-off - Replaced by o.c



$i(t) = 0$

$V_0 = i(t) R_L = 0$

$$\boxed{V_D = -V(t) = -V_m \sin\omega t}$$

* The max. voltage across 'D' = $-V_m$
* The max Reverse bias voltage across the diode is called "Peak inverse voltage".

$$\boxed{PIV = V_m}$$

→ The average value : $\boxed{\frac{V_m}{\pi} \text{ or } \frac{I_m}{\pi}}$

→ RMS value : $\boxed{\frac{V_m}{2} \text{ or } \frac{I_m}{2}}$

→ Efficiency $\eta = \left(\frac{0.406}{1+\frac{R_f}{R_L}}\right)$

$$\boxed{\eta_{max} = 40.6\%}$$

→ Ripple factor = $\frac{\text{AC component present in o/p}}{\text{DC component present in o/p}}$

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{avg}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21$$

→ indicates more ac comp (1.21 times) than DC components, but we want DC o/p, η is poor.

Advantage:-

1. circuit is simple

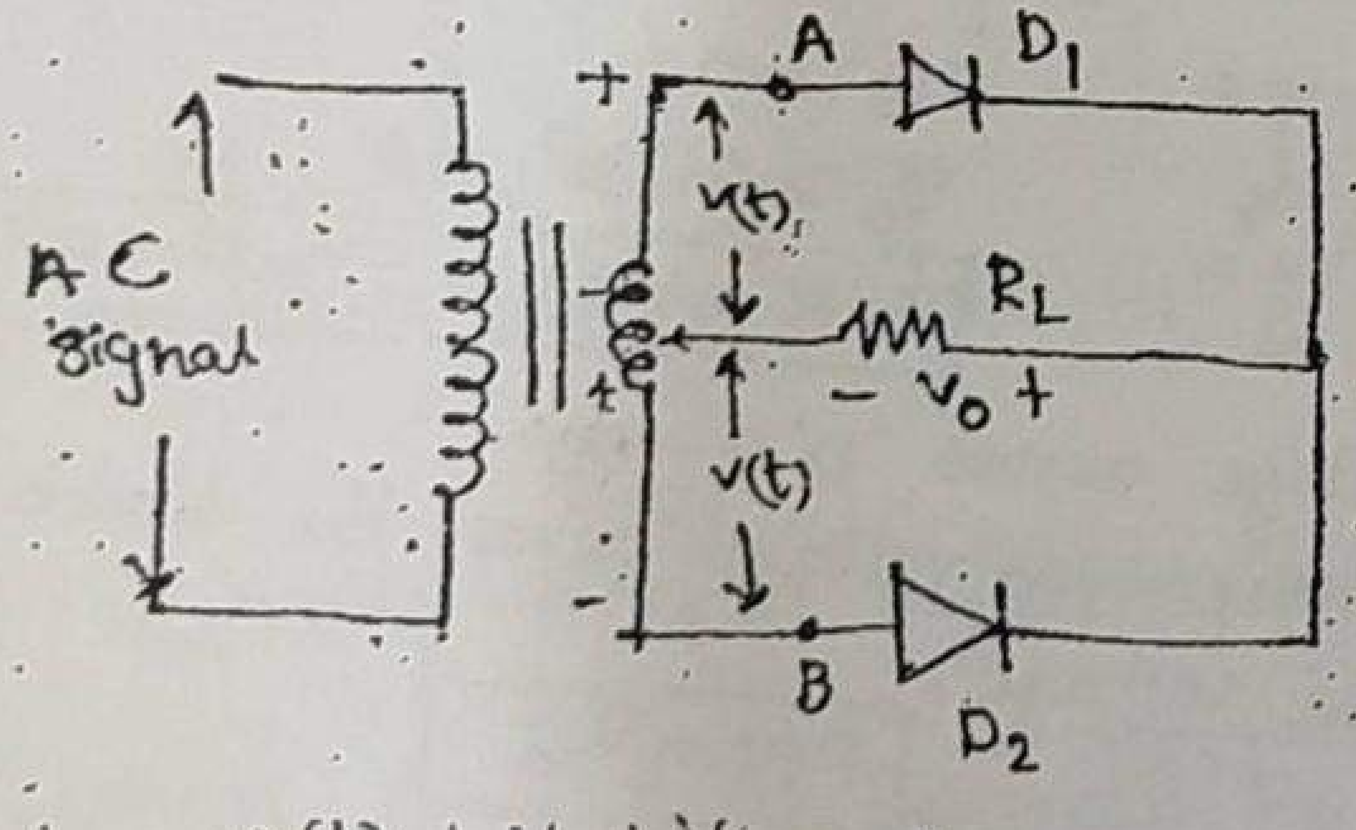
Disadvantage:-

1. Efficiency is less
2. $\gamma > 1$

* To overcom the disadvantages of halfwave rectifier we use full wave rectifiers.

Fullwave Rectifier:-

1. Centre tapped FWR:-



$$v(t) + V_0 + V_{D2} = 0$$

$$V_{D2} = -[v(t) + V_0]$$

$$= -2V_m \sin\omega t$$

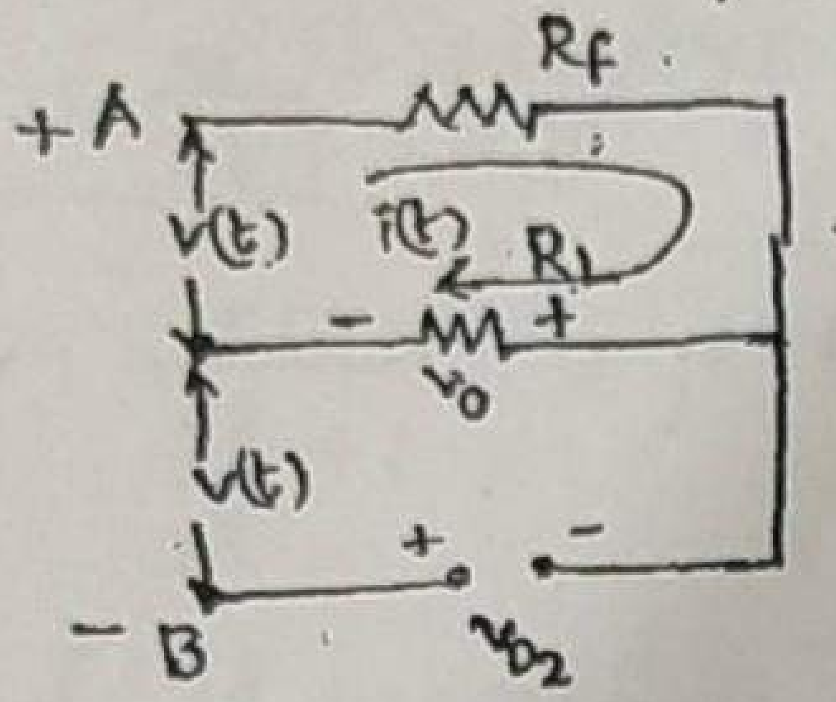
↓ D_2 R.B

$$\boxed{(PIV)_{D2} \simeq 2V_m}$$

During +ve cycle:-

A +ve D_1 ON by R_f

B -ve D_2 off by O.C



$$i(t) = \frac{v(t)}{R_f + R_L}$$

$$= \frac{V_m}{R_f + R_L} \sin\omega t$$

$$\boxed{i(t) = I_m \sin\omega t}$$

$$V_{D_1} = i(t) R_f$$

$$= I_m R_f \sin\omega t$$

$$V_0 = i(t) R_L$$

$$= V_m \left(\frac{R_L}{R_f + R_L}\right) \sin\omega t$$

$$\boxed{V_0 \simeq V_m \sin\omega t}$$

$V_{D_2} = ?$ apply KVL in lower half.

$$v(t) + V_0 + V_{D_2} = 0$$

$$V_{D_2} = -[v(t) + V_0]$$

$$= -2V_m \sin\omega t$$

↓

D_2 R·B

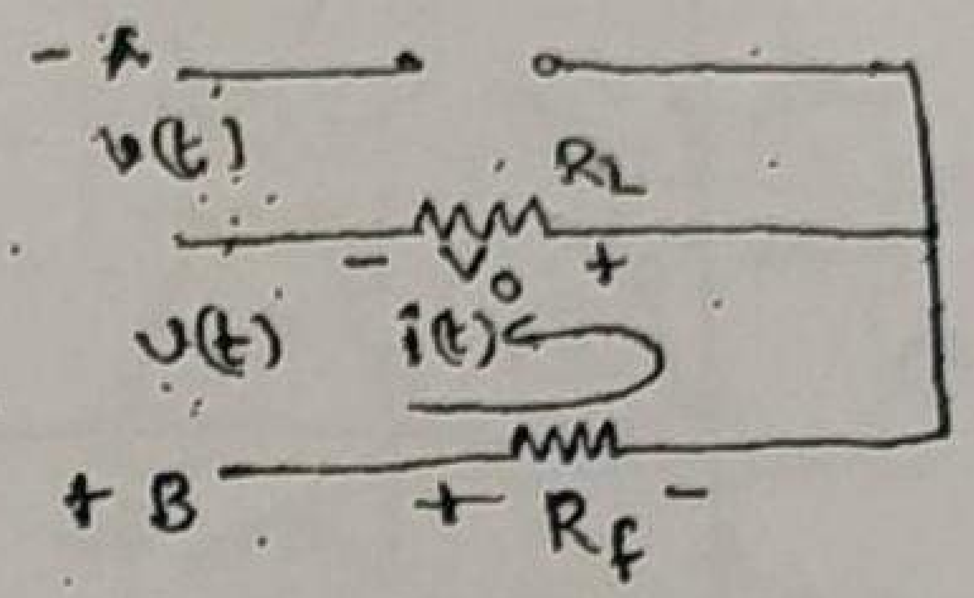
$$\boxed{(PIV)_{D_2} \simeq 2V_m}$$

Chinu

During -ve cycle:-

A -ve D_1 - OFF → O.C

B +ve D_2 - ON → by R_f



$$i(t) = \frac{v(t)}{R_f + R_L}$$

$$i(t) = I_m \sin\omega t$$

$$V_{D2} = i(t) R_f$$

$$= I_m R_f \sin\omega t$$

$$V_0 = i(t) R_L$$

$$V_0 \simeq V_m \sin\omega t$$

$$V_{D1} \simeq -2V_m \sin\omega t$$

$$V_{D_1} \simeq \boxed{(PIV)_{D_1} \simeq 2V_m}$$

Advantages

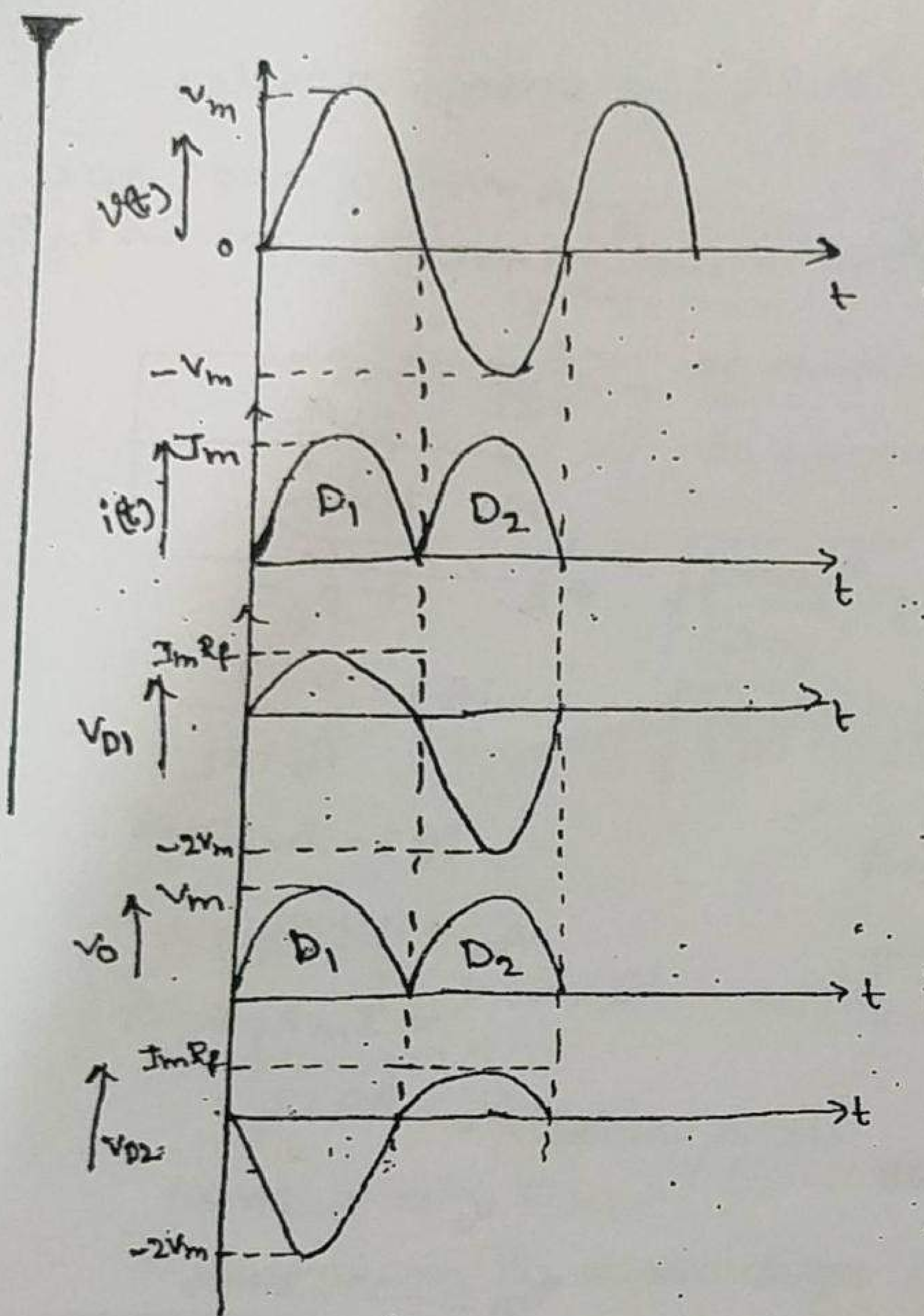
(1.) η of FWR is twice that of HWR

(2.) $\Gamma < 1$.

Disadvantages:-

1. $PIV = 2V_m$
2. centre tapping is difficult.

⇒ To overcome the disadvantages of centre tapped we use bridge Rectifier.



1) Avg value $= \boxed{\dfrac{2V_m}{\pi} \text{ \& } \dfrac{2I_m}{\pi}}$

2) RMS value $= \boxed{\dfrac{V_m}{\sqrt{2}} , \dfrac{I_m}{\sqrt{2}}}$

3) $\eta = \dfrac{0.812}{1+\dfrac{R_f}{R_L}}$ (2 times HWR)

$\therefore \eta_{max} = 81.2\%$

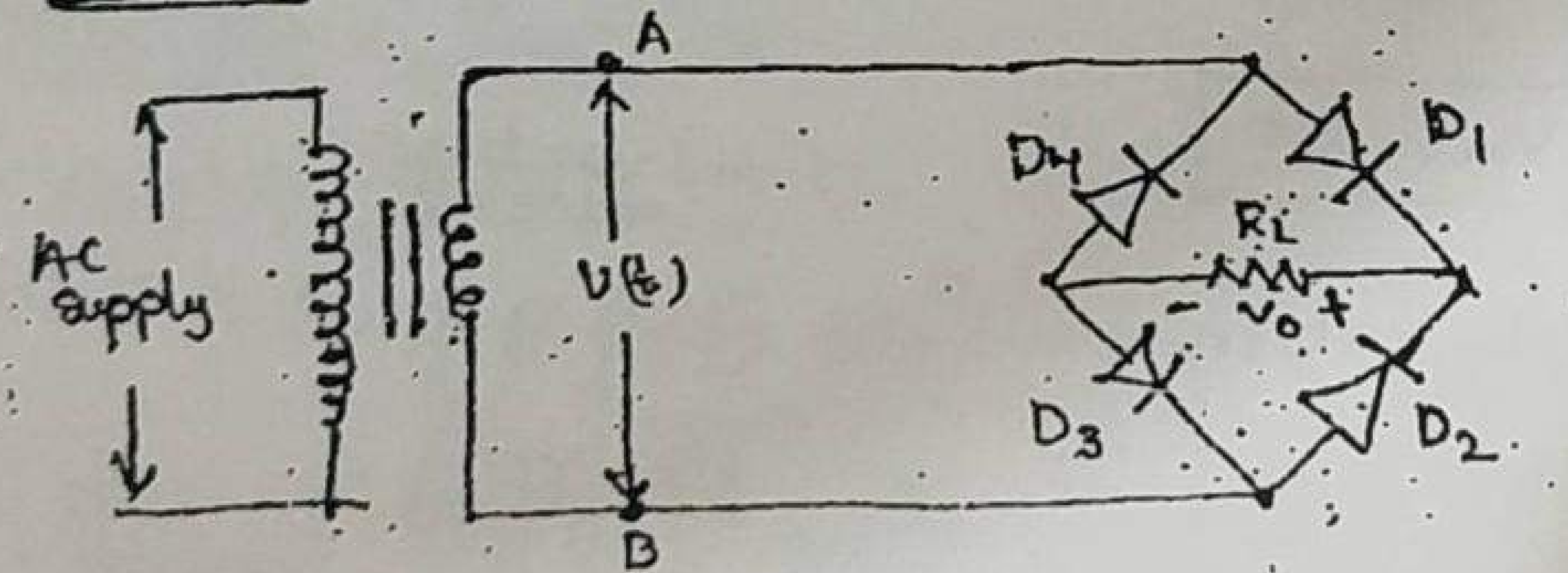
4) Ripple factor $= \sqrt{\left(\dfrac{V_{rms}}{V_{avg}}\right)^2 - 1}$

$= \sqrt{\left(\dfrac{\pi}{2\sqrt{2}}\right)^2 - 1}$

$= 0.483$

5) $PIV = 2V_m$.

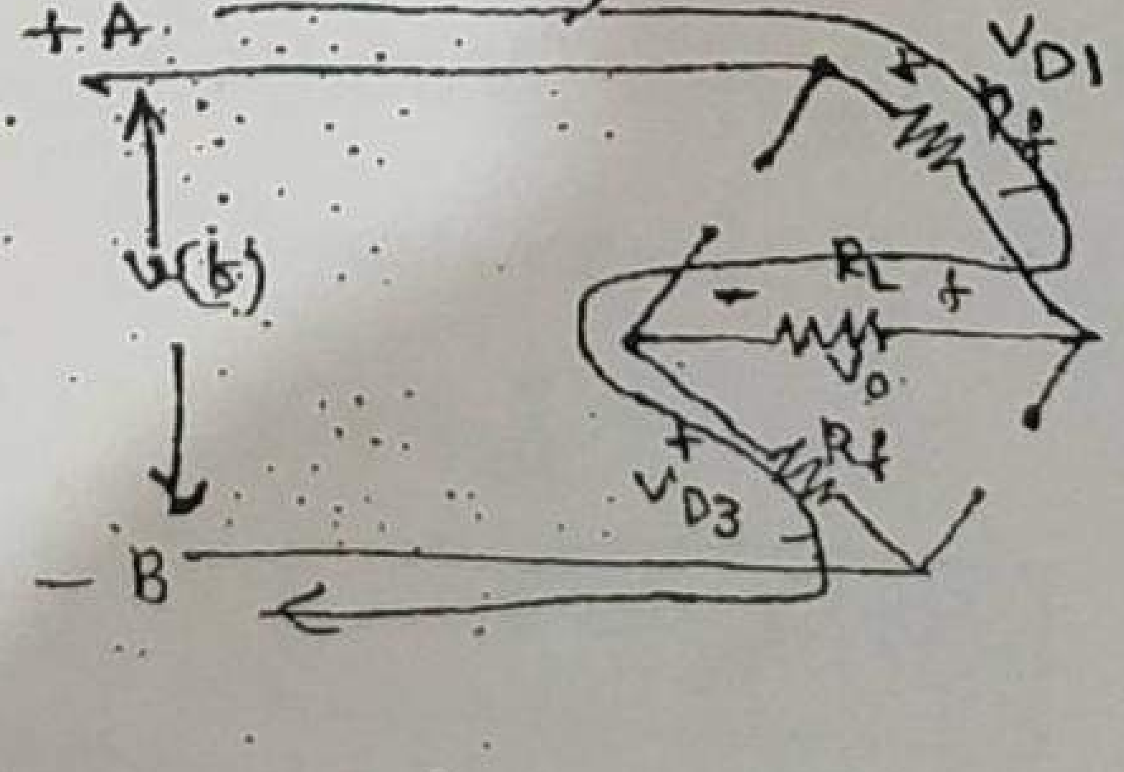
BRIDGE RECTIFIER:-



During +ve cycle of $v(t)$:-

$\therefore$ A → +ve → D_1-ON, D_4-off

B → -ve → D_3-ON, D_2-off



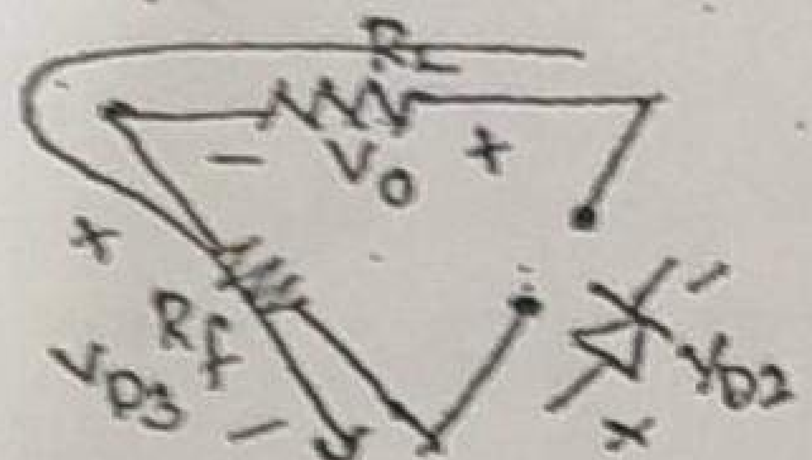
$i(t) = \dfrac{V_m}{2R_f + R_L} \sin\omega t$

$= I_m \sin\omega t$

$V_{D1}, V_{D3} = i(t) R_f$

$= I_m R_f \sin\omega t$; $V_0 \simeq V_m \sin\omega t$, $R_L >> R_f$

To calculate V_{D2} consider lower half Bridge:



$$V_{D2} + V_0 + V_{D3} = 0$$

$$V_{D2} = -\left[V_0 + V_{D3}\right]$$

$$= -\left[\frac{V_m R_L}{2R_f + R_L} + \frac{V_m R_f}{2R_f + R_L}\right] \sin\omega t$$

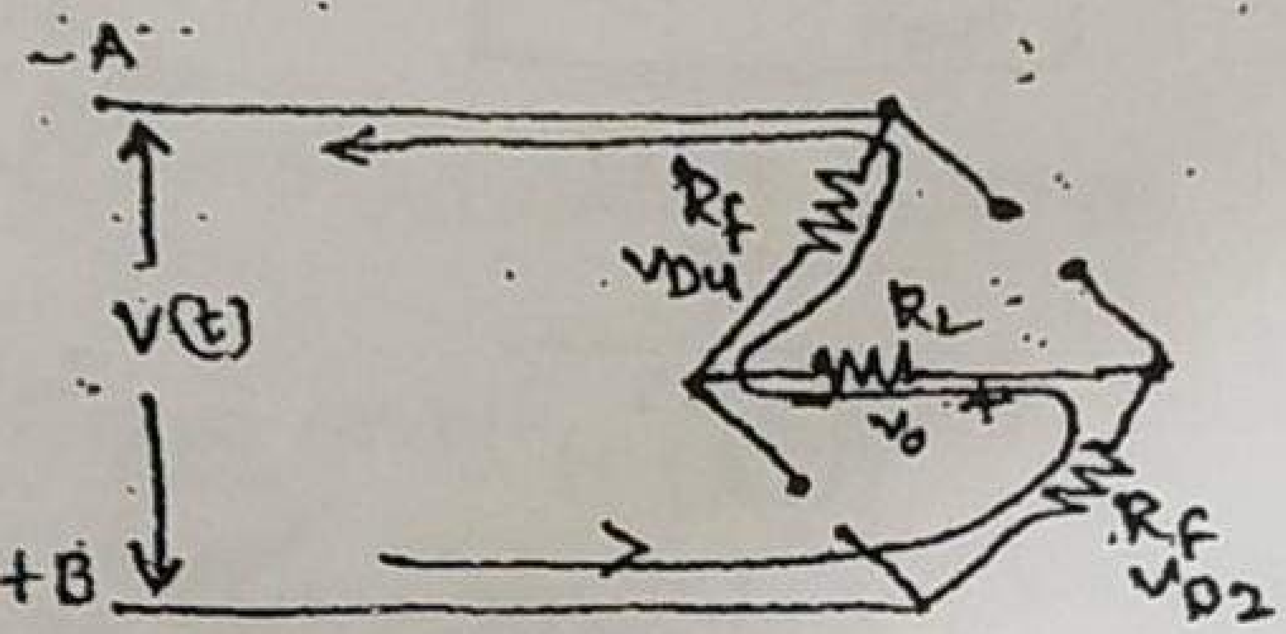
$$= \frac{-V_m}{2R_f + R_L}(R_L + R_f)\sin\omega t$$

$$V_{D2} \simeq -V_m \sin\omega t$$

Similarly $V_{D4} \simeq -V_m \sin\omega t$

$$\boxed{(PIV)_{D2, D4} \simeq V_m}$$

<u>During -ve cycle of V(t)</u>:-



B → +ve → D_2-ON, D_3-off

A → -ve → D_4-ON, D_1-off

$$V_0 = V_m \sin\omega t$$

$$V_{D2} = V_{D4} = I_m \sin\omega t \, R_f$$

$$V_{D3} = V_{D1} = ?$$

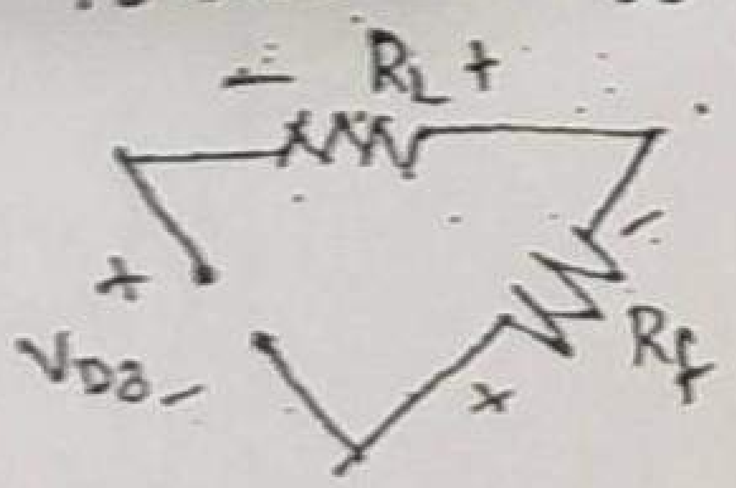
$$i(t) = \frac{V_m}{2R_f + R_L}\sin\omega t = I_m \sin\omega t$$

$$V_0 = i(t) R_L$$

$$= V_m \frac{R_L}{(2R_f + R_L)} \sin\omega t$$

$$V_0 \simeq V_m \sin\omega t \quad R_L >> R_f$$

To calculate V_{D3} consider lower half bridge.



$$V_{D2} + V_0 + V_{D3} = 0$$

$$V_{D3} = -\left[V_0 + V_{D2}\right]$$

$$V_{D3} = -\left[\frac{V_m R_L}{2R_f + R_L} + \frac{V_m R_f}{2R_f + R_L}\right] \sin\omega t \simeq -V_m \sin\omega t.$$

Similarly $V_{D1} = -V_m \sin\omega t$.

$$\boxed{(PIV)_{D_1, D_3} = V_m}$$

1. Average value:-

$= \frac{2V_m}{\pi}$ (or) $\frac{2I_m}{\pi}$

2. RMS value:-

$= \frac{V_m}{\sqrt{2}}$ (or) $\frac{I_m}{\sqrt{2}}$

3. Efficiency:-

$\eta = \left(\frac{0.812}{1+2\frac{R_f}{R_L}}\right)$

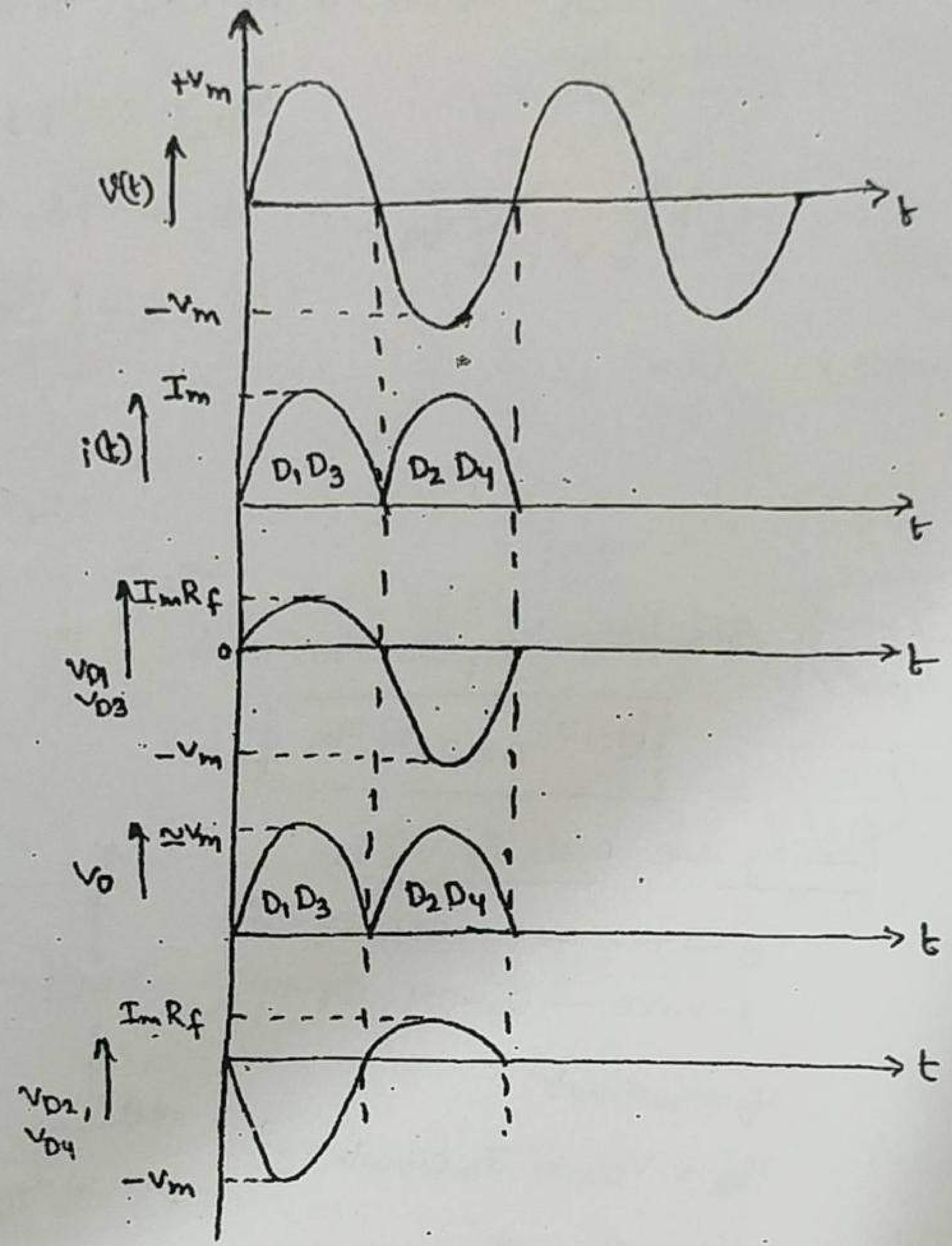
$\boxed{\eta_{max} = 81.2\%}$

4. Ripple factor:-

$r = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$

$= 0.483$

5. PIV = V_m.



Advantages:-

1. η of FWR is twice that of HWR
2. $r < 1$
3. No necessity of centre tapping
4. PIV = V_m

$\therefore$ Bridge Rectifier is more efficient to convert AC signal into pulsating DC.

Disadvantage:-

1. No. of diodes required 4.

Zener Diode Characteristics:-

purpose:-

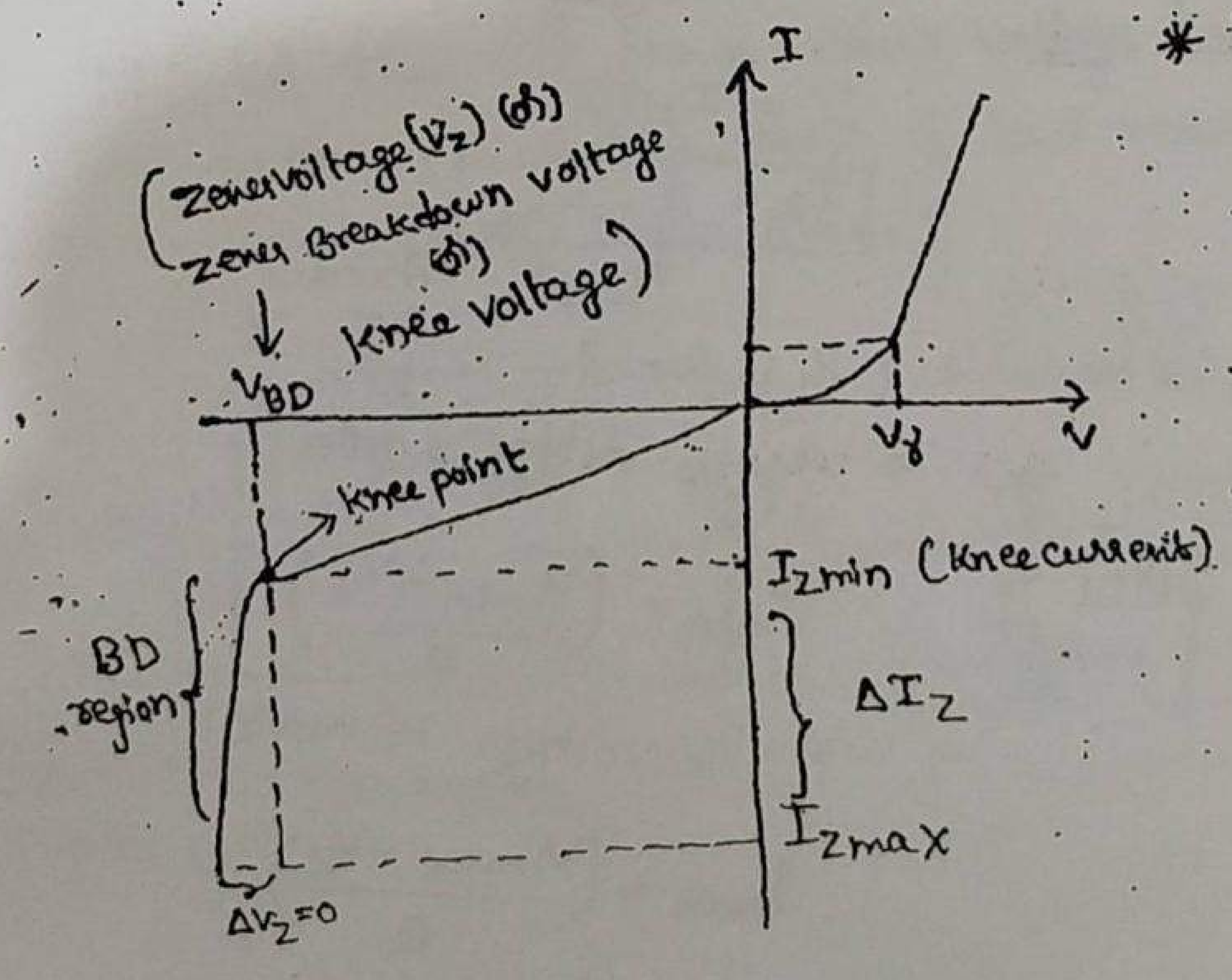
1. To operate in the reverse bias region.
   To conduct the currents in the order of mA in R.B region
2. To withstand for large generation of temperature.
   Once breakdown occurs, uniform electric field across the Junction & it maintains constant voltage across its terminals i.e acts as Voltage Regulation.
3. The Breakdown voltage of Zener is less than that of PN Junction diode. ∴ T ⇒ max temp.
4. zener diode is heavily doped compared to PN Junction diod

   Doping levels:- $1:10^6$

   $100 : 10^8$ → Intrinstic atoms.

   (100 →) doped atoms
5. zener diodes are of silicon type only.

⇒ A heavily doped si diode which has sharp breakdown voltage is called zener diode. when Zener diode is F.B → acts as normal PN Junction diode of si type.

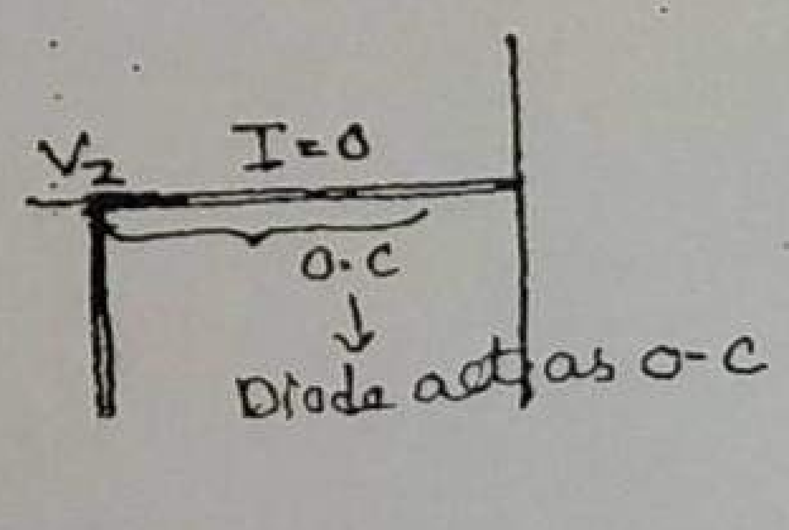


* Dynamic resistance of zener:

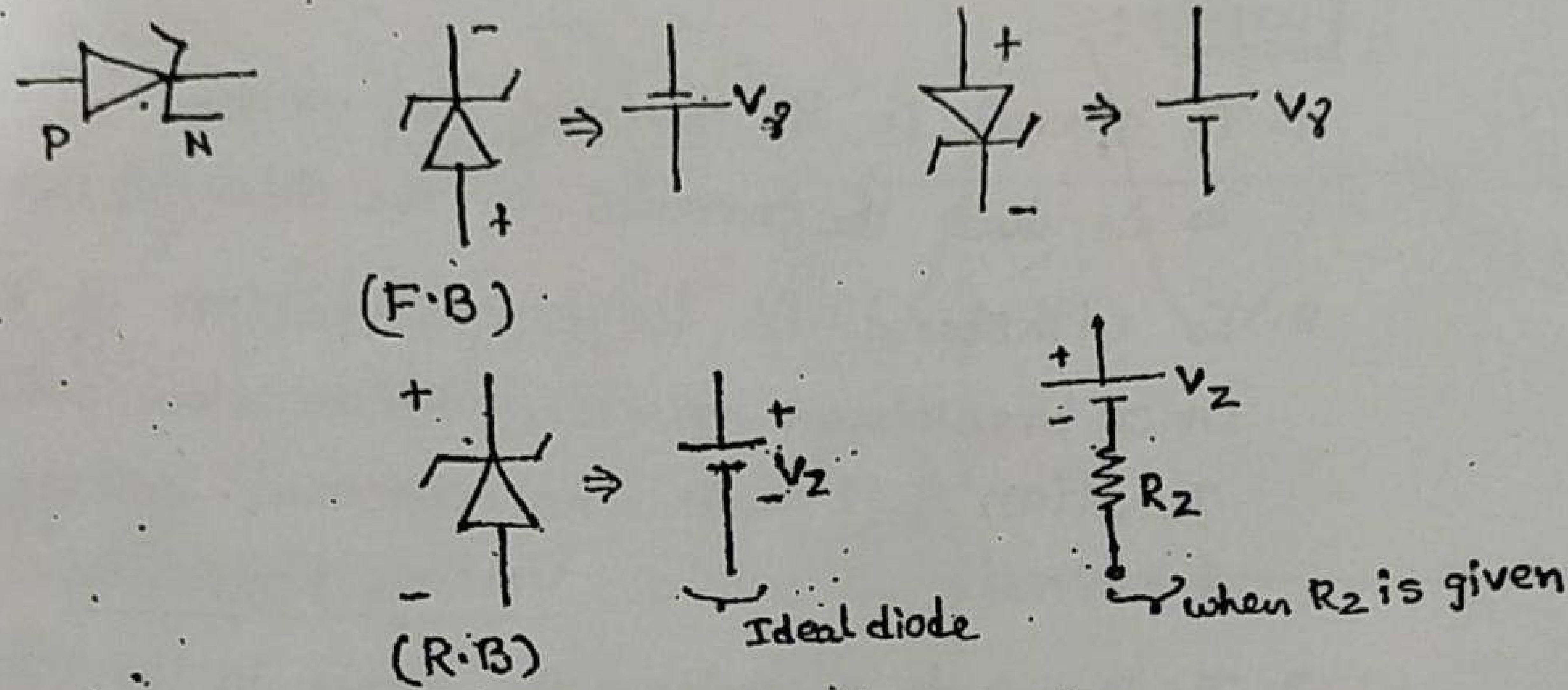
$$R_Z = \frac{\Delta V_Z}{\Delta I_Z} \rightarrow \text{very small}$$

Ideal zener $\left.\begin{array}{l}\Delta V_Z = 0 \\ R_Z = 0\end{array}\right\}$ Ideal diode

* when I_{Zmin} is not given, consider $\boxed{I_{Zmin} = 0}$

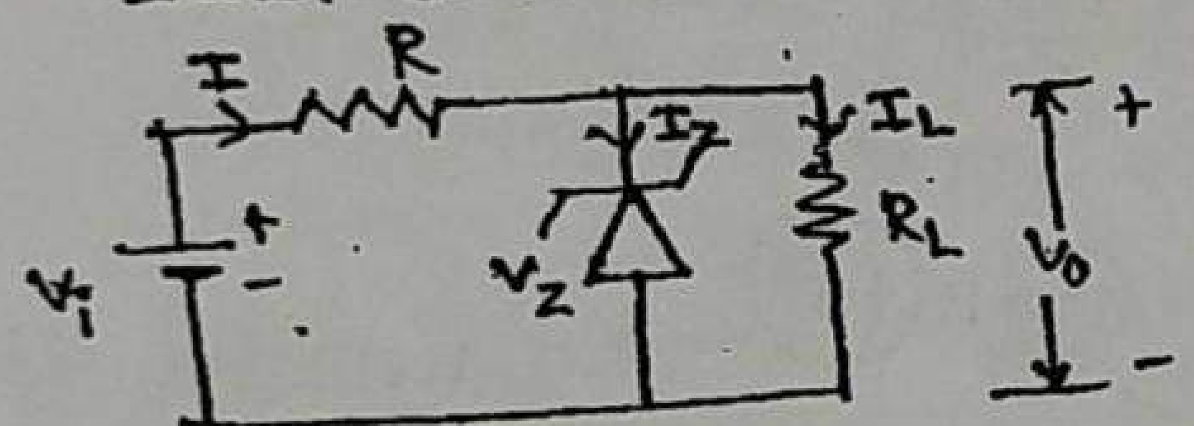


Zener equivalent ckt:-



Zener diode as voltage Regulator:-

Zener diode must operate in the Breakdown region.

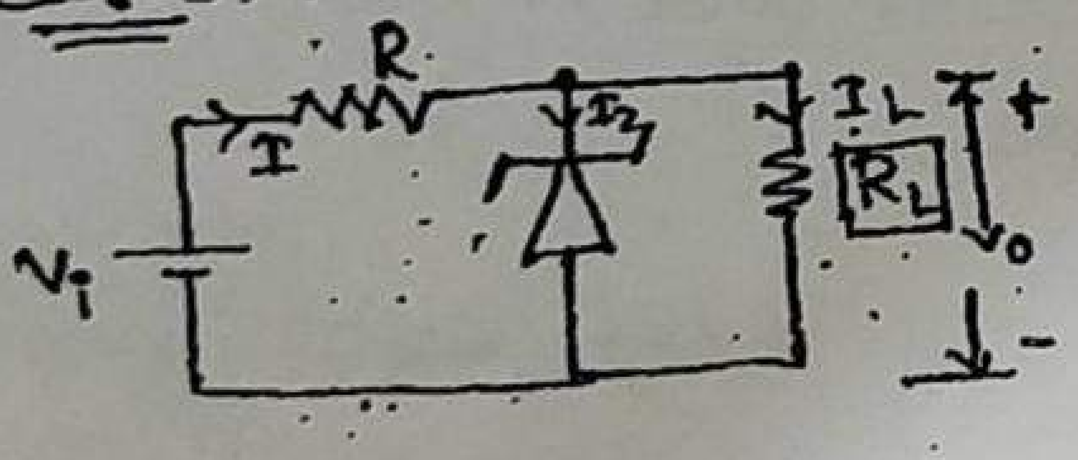


$\rightarrow V_i > V_z$

$$\boxed{I = I_z + I_L}$$

A voltage regulation is a ckt which maintains constant voltage across its terminals even V_i (or) R_L varies.

Case(i): when V_i & R_L are constant



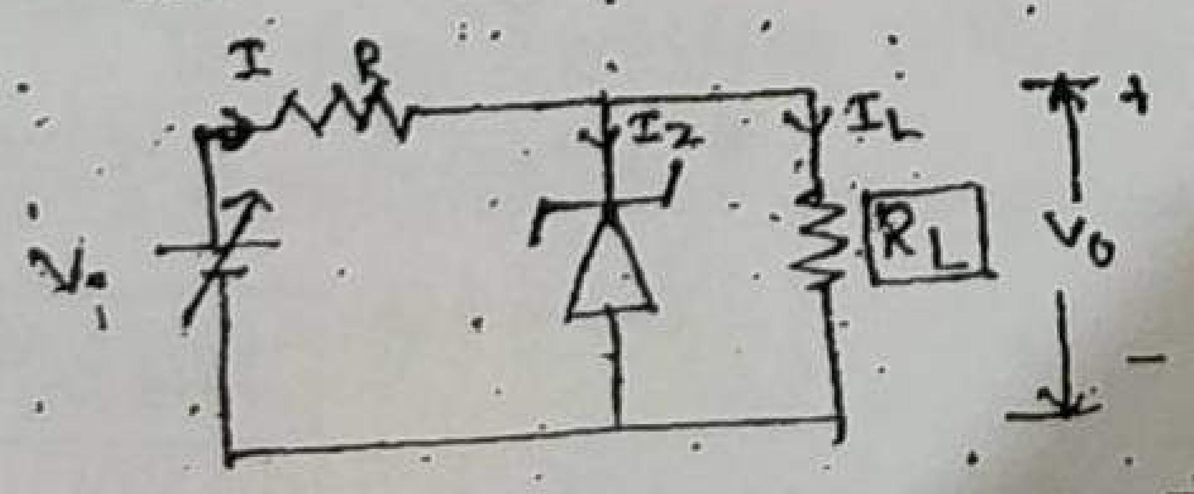
$\Rightarrow I_L = \frac{V_0}{R_L} = \frac{V_z}{R_L} \rightarrow$ fixed

$I = \left(\frac{V_i - V_z}{R}\right) \rightarrow$ fixed

$I = I_z + I_L$

$$\boxed{I_z = \underbrace{I}_{\text{fixed}} - \underbrace{I_L}_{\text{fixed}}}$$

Case(ii): when V_i is variable & R_L is fixed



$\rightarrow$ when i/p voltage is min

$$I_{min} = \left(\frac{V_{imin} - V_z}{R}\right)$$

$\rightarrow$ when i/p voltage is max

$$I_{max} = \left(\frac{V_{imax} - V_z}{R}\right)$$

$$\boxed{\begin{aligned} I_{zmin} &= I_{min} - I_L \\ I_{zmax} &= I_{max} - I_L \end{aligned}}$$

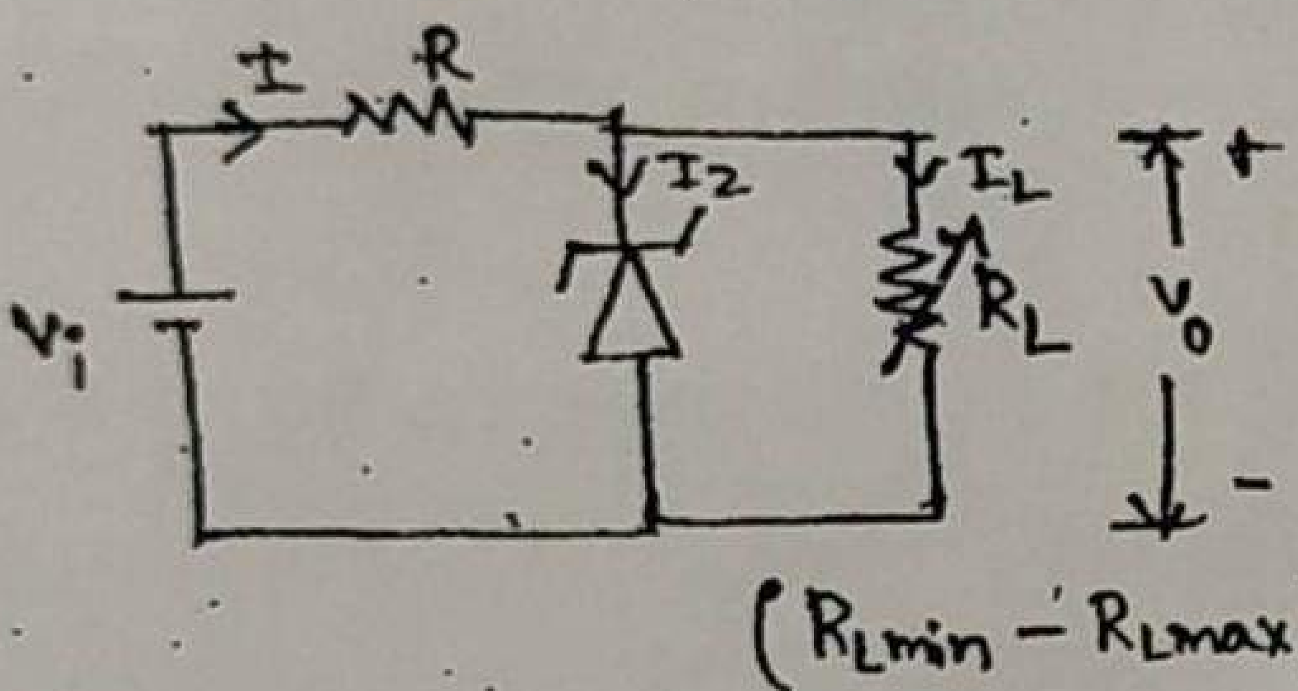
$$I_L = \frac{V_0}{R_L} = \frac{V_z}{R_L} \rightarrow \text{fixed}$$

$$\boxed{I_z = I - \underbrace{I_L}_{\text{fixed}}}$$

$V_i\uparrow$ $I\uparrow$ $I_z\uparrow$

$V_i\downarrow$ $I\downarrow$ $I_z\downarrow$

case iii: when V_i fixed & R_L variable:



$(R_{Lmin} - R_{Lmax})$

$$\therefore I_{Lmin} = \frac{V_z}{R_{Lmax}}$$

$$\therefore I_{Lmax} = \frac{V_z}{R_{Lmin}}$$

$$I = \left(\frac{V_i - V_z}{R}\right) \rightarrow \text{Fixed}$$

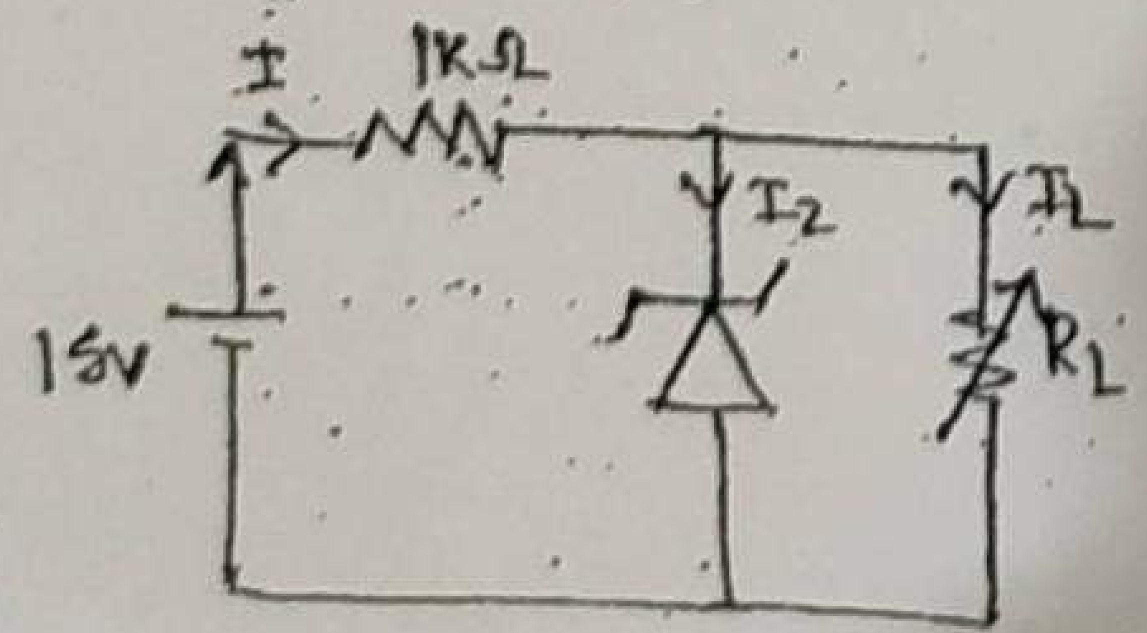
$$\boxed{I_z = \underbrace{I}_{\text{fixed}} - I_L}$$

$R_L\uparrow$ $I_L\downarrow$ $I_z\uparrow$

$R_L\downarrow$ $I_L\uparrow$ $I_z\downarrow$

$$\boxed{\begin{aligned} I_{zmax} &= I - I_{Lmin} \\ I_{zmin} &= I - I_{Lmax} \end{aligned}}$$

pb:- For the ckt shown zener voltage is 8v, zener currents are 2mA to 5mA, find the range of load resistance for satisfactory operation of zener diode?



$$I = \frac{15-8}{1K} = 7mA$$

$$I_{zmin} = 2mA$$

$$I_{zmax} = 5mA.$$

TRANSISTOR :-

* Transistor Fundamentals:-

TRANS / ISTOR

TRANS → Transfer of

ISTOR → Resistance

→ Transfers the signal from one resistance level to another resistance level i.e signal transferred from i/p port to o/p port.

→ while transfering the (or) signal from i/p port to o/p port it does the amplification process.

→ Depending on conduction of current due to charged particles ($\bar{e}$ & holes) transistors are classified into:

1. Bipolar transistor.
2. Unipolar transistor.

⇒ Bipolar transistor:

* The current conduction due to both $\bar{e}$ & holes

  Ex:- BJT

* Depending on construction principle BJT classified into

  1. NPN transistor
  2. PNP transistor

The mobility of $\bar{e}$ (μ_n) is greater than that of holes (μ_p) i.e $\mu_n \simeq 2.6\mu_p$

* The conductivity in NPN transistor is more than that in PNP transistor.

* NPN transistors are preferably used compared to PNP.

* BJT is a current Controlled device. i.e the o/o current is controlled by the i/p current.

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* o/p current depends on i/p current.

$$\boxed{\text{o/p current} = f_{un}[\text{i/p current}]}$$

⇒ unipolar transistor:-

* The current conduction due to either $\bar{e}$ & holes.

  Ex: FET.

* The current conduction due to only $\bar{e}$ – N channel FETs

  The current conduction due to only holes – P channel FETs

N channel FETS are preferably used compared to p channel FETS.

- Depending on the construction principle FETS are classified into:

  1. JFET
  2. MOSFET (or) Insulated gate FET (IGFET)

     - Enhancement MOSFET
     - Depletion MOSFET.

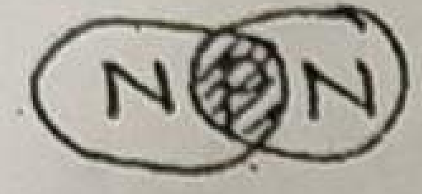
* FET is a voltage controlled device.

ie the o/p current is controlled by the applied i/p voltage.

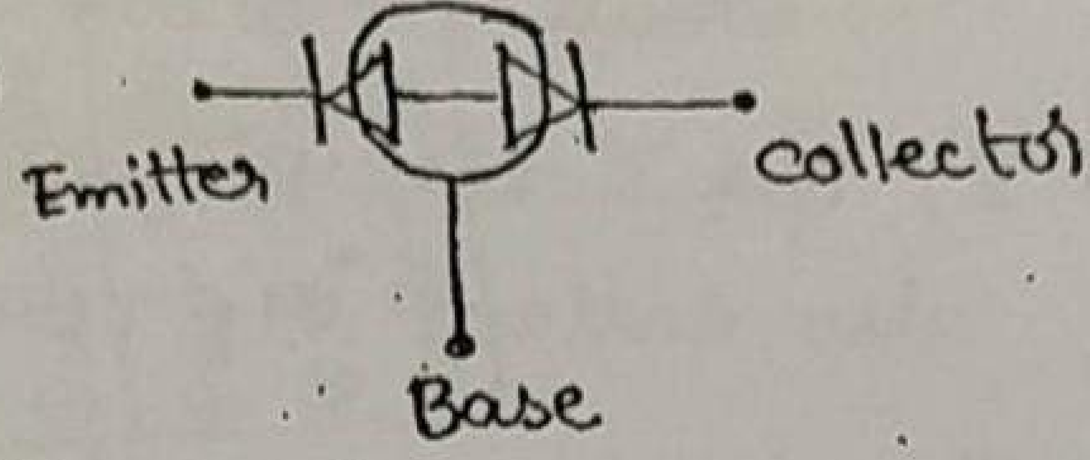
$$\boxed{\text{o/p current} = f[\text{i/p Voltage}]}$$

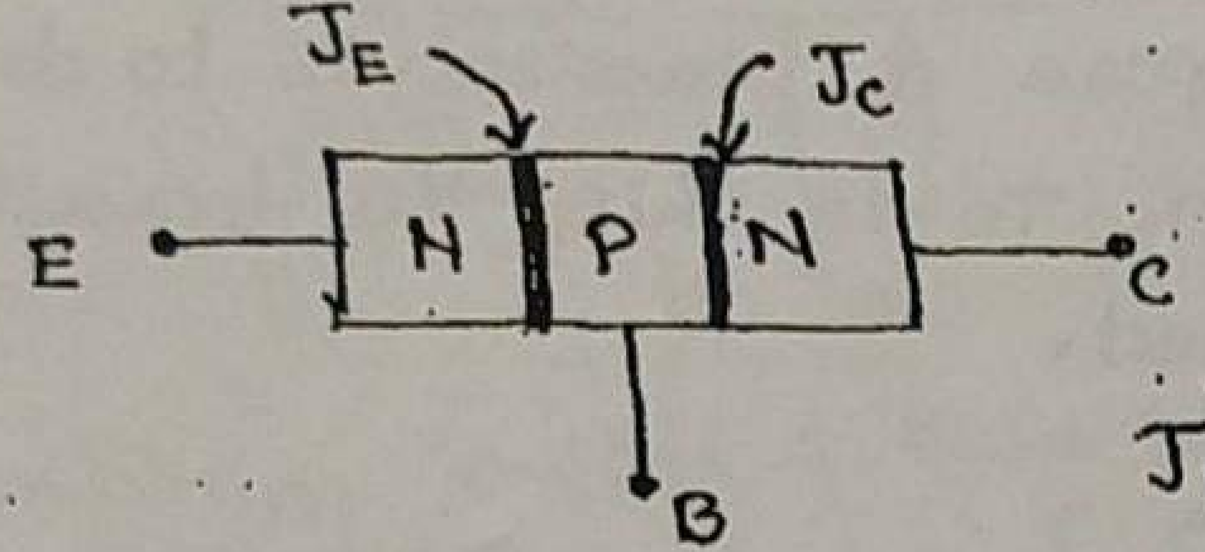
* FET is a low Noise device compared to BJT.

Bipolar Junction Transistor :- (BJT)



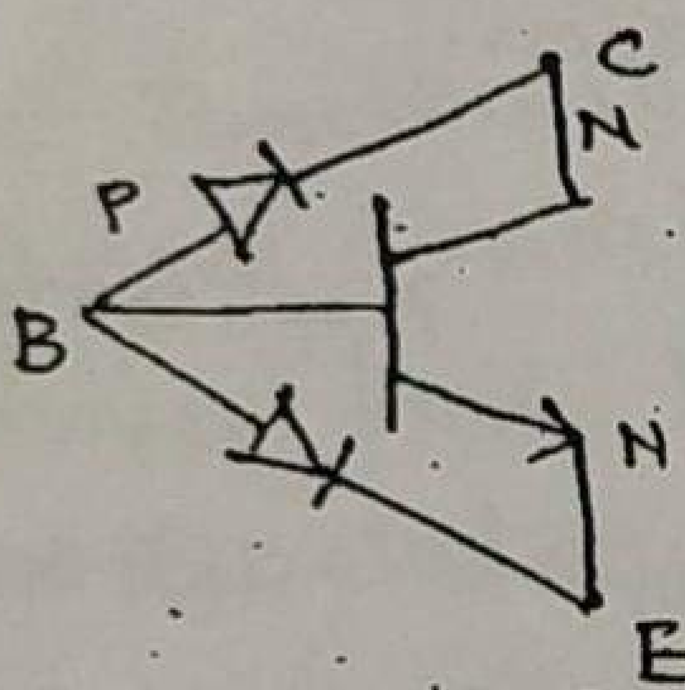
Transistor



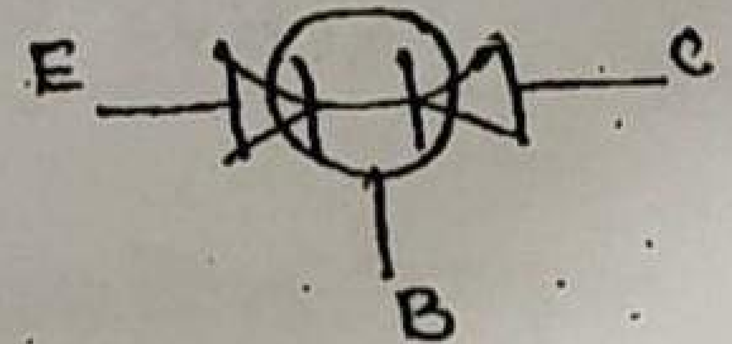


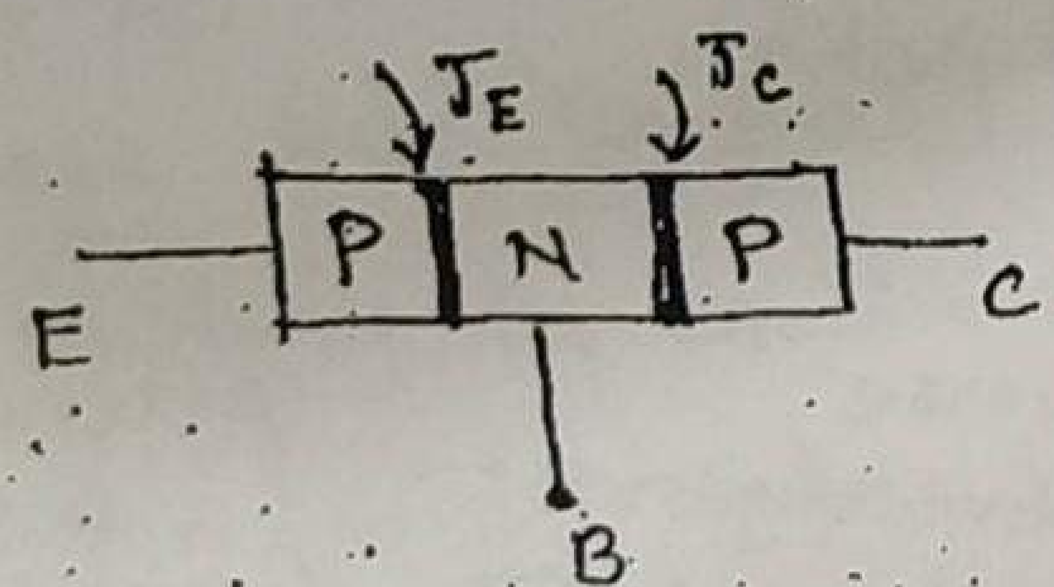
J_E → Emitter - Base Junction (or) Emitter Jun.

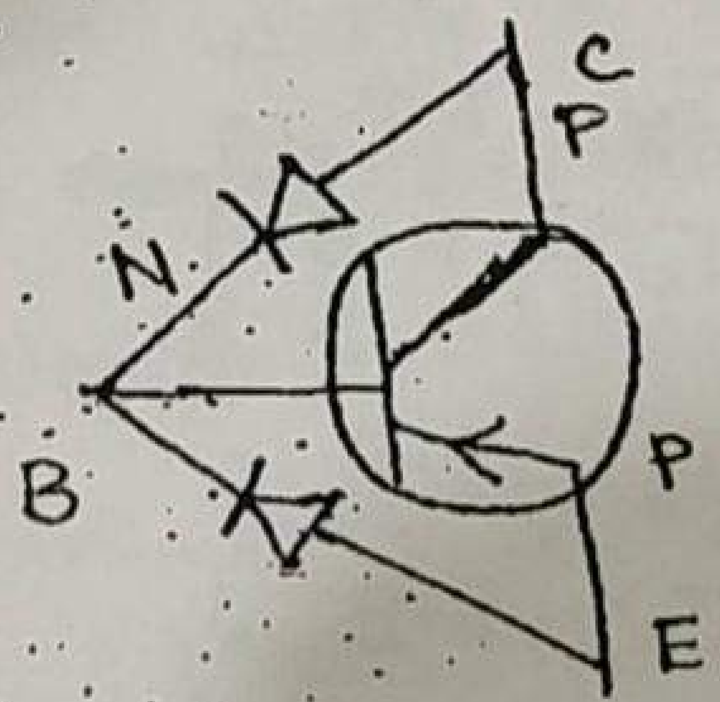
J_c → collector - Base Junction (or) collector Jun.



PNP transistor :-







Emitter:- To emit the charged particles.

- Heavily doped.
- Medium in size.

Collector: To collect the charged particles which are emitted by emitter.

- Moderately doped.
- Large in size.

Base: To control the current through the transistor
- Lightly doped.
- small in size.

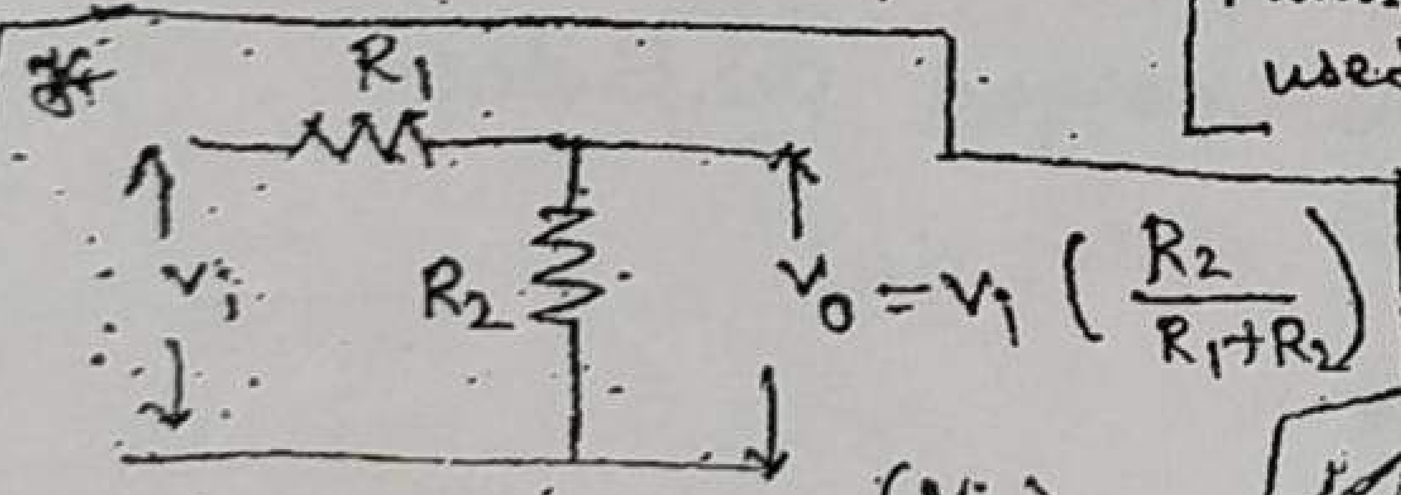
* 'E', 'B' & 'C' are unequally doped. So that the BJT is also called "HETERO JUNCTION DEVICE"

* The main purpose of transistor is to do the faithful amplification. To do this, the transistor must be properly biased.

i.e $\left.\begin{array}{l} J_E - F.B \\ J_C - R.B \end{array}\right\} \rightarrow$ Active Region.

Junctions	Region of operation	Application
J_E - R.B, J_C - R.B $\rightarrow$	cutt off Region	OFF switch.
J_E - F.B, J_C - R.B $\rightarrow$	Active Region	Amplifier.
J_E - F.B, J_C - F.B $\rightarrow$	Saturation	ON switch.
J_E - R.B, J_C - F.B $\rightarrow$	Inverse Active region [Transistor never used in this region]	Attenuator. (reduce the amplification)

*



$\left(\frac{v_i}{I_0}\right)$

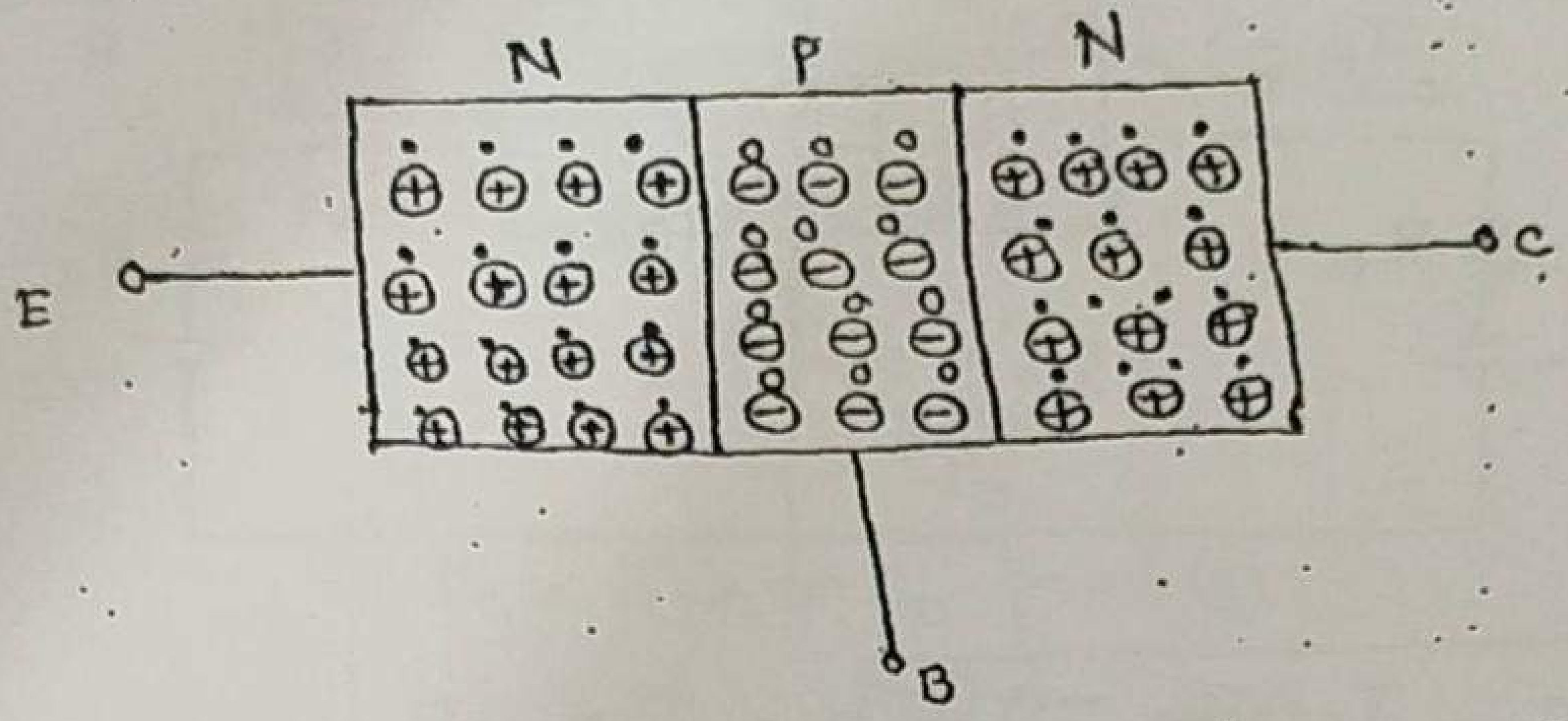
$R_2 : R_1 = 1:9$

The Attenuator process will done at low cost in this ckt (Resistor)

(Reason is this)

$\Rightarrow$ So the transistor will not do the Attenuator process.

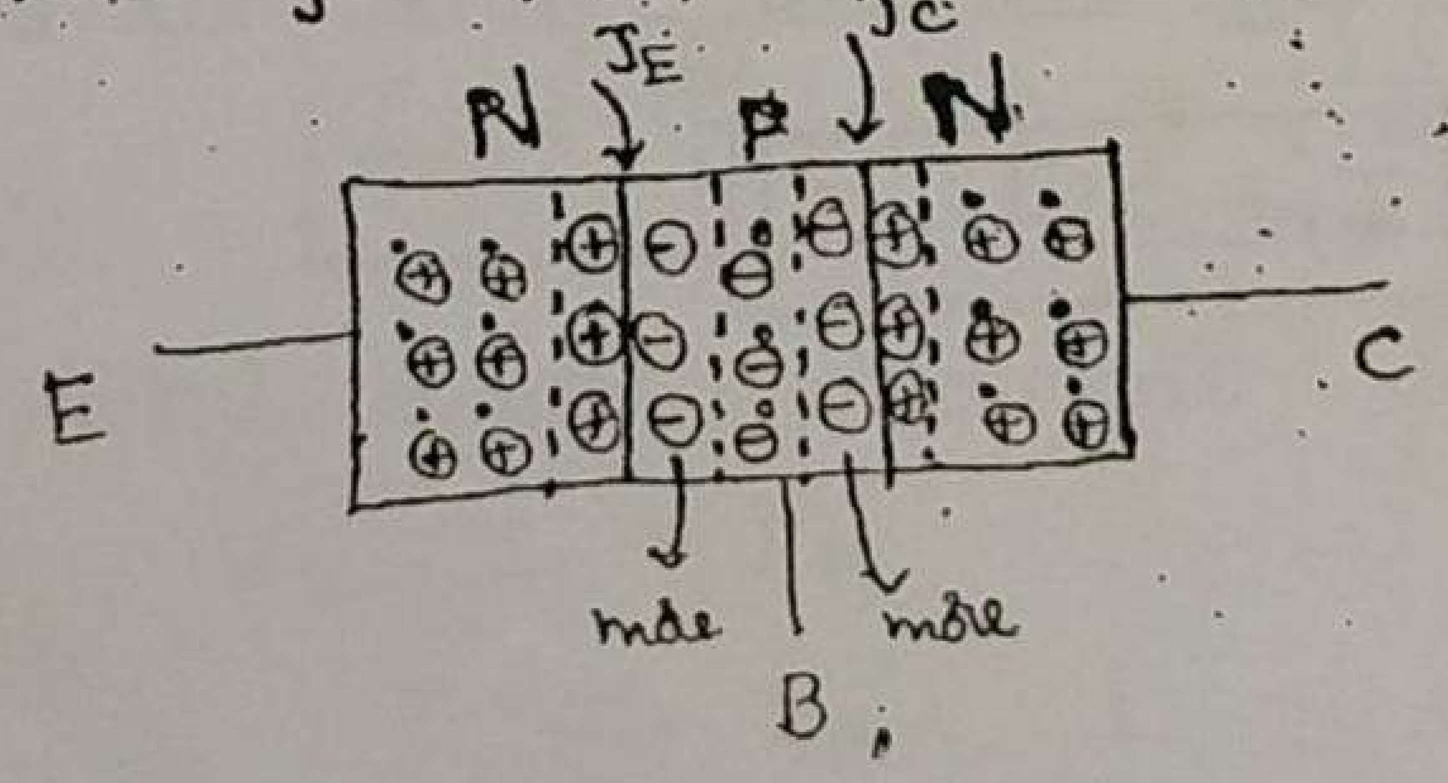
Depletion region Formation:-



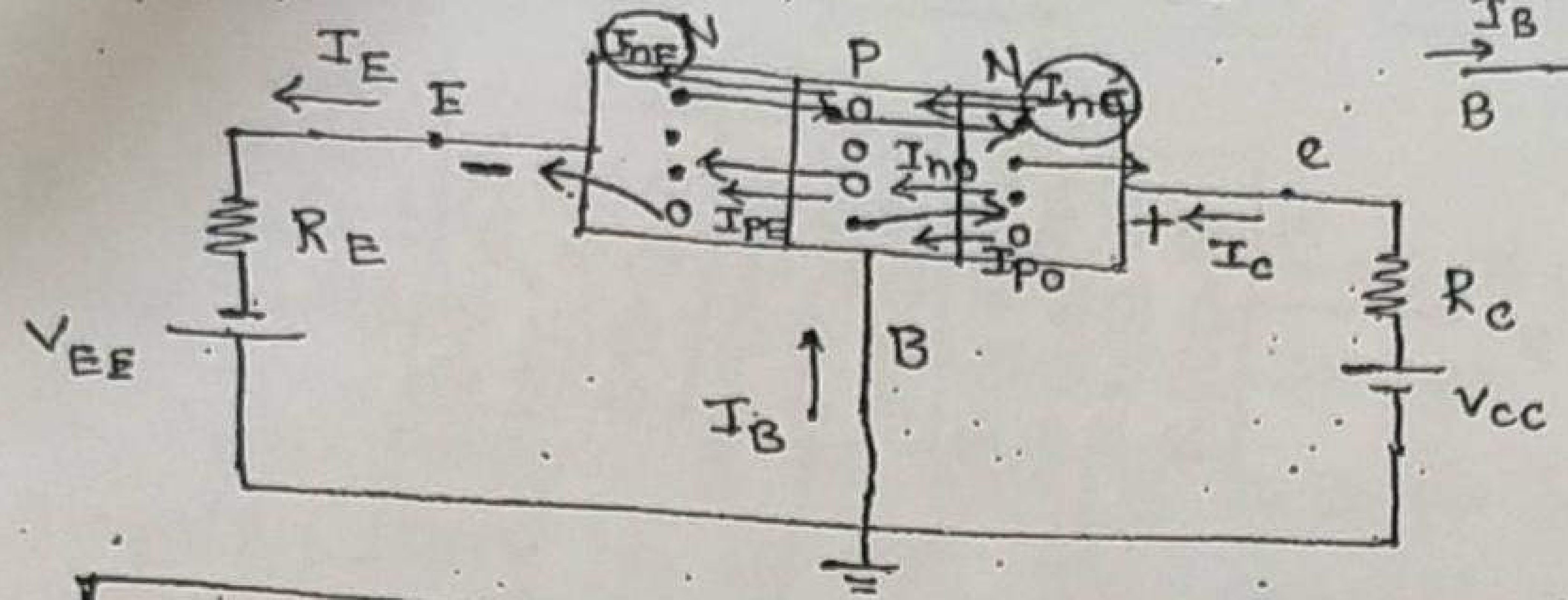
By combining emitter & Base a small force acting on the Junction (J_E) this force causes motion in the charged particles, these charged particles always moves from higher concentration to lower concentration i.e the electrons moves from n-type to p-type & holes moves from P-type to N-type. to this recombination takes place in both the regions as emitter is heavily doped compared to base the recombination rate is more in base side compared to emitter side.

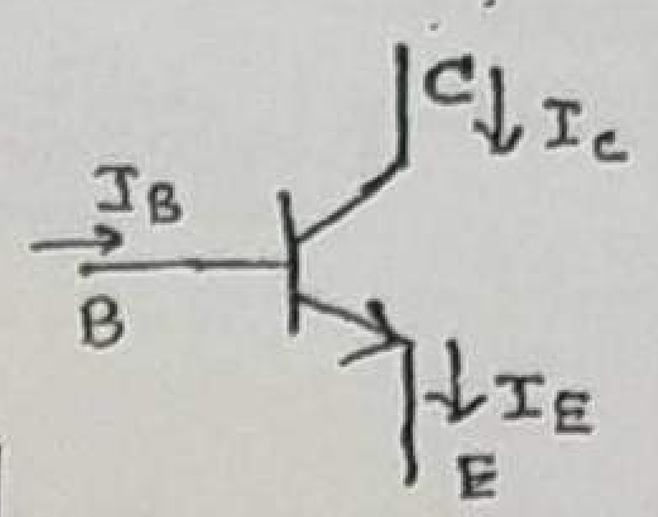
So that the depletion region width is more into Base side compared it to emitter side.

Similarly By combining collector & Base the depletion region width more into base side compared to collector side. simply in the transistor the depletion region width more into lightly doped side compared to heavily doped side.



Current components in Transistor :-





$$\boxed{I_E = I_c + I_B} \rightarrow ①$$

1. I_{nE} → current due to $\bar{e}$ [which are majority carries of E] and it flows into 'E' region.
2. All the minority carriers of 'E' moves away from 'J_E'. They cannot form loop. $(I_{minority})_E = 0$.
3. I_{PE} → current due to holes [which are majority carries of Base) & it flows into 'E' region.
4. I_{no} – current due to electrons [which are minority carriers of Base] & it flows from 'C' to B region.
5. All the maj carriers of 'C' moves away from 'J_c'. They cannot from loop. $(I_{maj})_c = 0$
6. I_{PO} – current due to holes (which are minority carriers of 'C') & it flows from 'C' to 'B'.
7. I_{nC} – current due to $\bar{e}$, due to collection of $\bar{e}$ by the collector from the emitter

$\therefore \boxed{I_{nE} > I_{nC}}$

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Apply KCL in Emitter.

$$\boxed{I_E = I_{nE} + I_{pE}} \rightarrow (2)$$

Apply KCL in Collector.

$$I_C = I_{nc} + \underbrace{I_{no} + I_{po}}_{I_0}$$

$$\boxed{\begin{array}{l} I_C = I_{nc} + I_0 \rightarrow (3) \\ I_0 = I_{no} + I_{po} \rightarrow (4) \end{array}}$$

* These 4 eq'n are called transistor Fundamental current equations.

Current gain 'α' (common Base):-

$$\alpha = \frac{\text{The injected maj carrier current at 'c'}}{\text{The total Emitter current}}$$

$$\boxed{\alpha = \left(\frac{I_{nc}}{I_E}\right) \text{ (or) } \frac{I_C - I_0}{I_E}}$$

$I_C = \alpha I_E + I_{CO}$

$$I_{nc} = \alpha I_E$$
$$= \alpha(I_C + I_B)$$

→ The total collector current is

$$I_C = I_{nc} + I_0$$
$$= \alpha(I_C + I_B) + I_0$$

$$I_C(1-\alpha) = \alpha I_B + I_0$$

$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_0}$$

$I_C = \beta I_B + (1+\beta) I_{CO}$

→ The total emitter current is

$$I_E = I_C + I_B$$
$$= \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_0 + I_B$$

$$= \left(\frac{\alpha}{1-\alpha}+1\right) I_B + \frac{1}{1-\alpha} I_0$$

$$\boxed{I_E = \frac{1}{1-\alpha}\left(I_B + I_0\right)}$$

when I_0 - Neglected,:-

$$I_{nc} = I_C$$

$$\boxed{\alpha = \frac{I_C}{I_E}} \text{ (or) } \boxed{I_C = \alpha I_E}$$

$$I_C = \alpha (I_C + I_B)$$

$$I_C(1-\alpha) = \alpha I_B$$

$$\boxed{I_C = \left[\frac{\alpha}{1-\alpha}\right] I_B}$$

$$\therefore I_E = I_C + I_B$$

$$= \frac{\alpha}{1-\alpha} I_B + I_B = \frac{1}{1-\alpha} I_B.$$

$$\boxed{I_E = \frac{1}{1-\alpha} I_B}$$

The relation b/w α & β is:

$$\alpha = \frac{\beta}{1+\beta} \quad \beta = \frac{\alpha}{1-\alpha}.$$

$$\frac{1}{1-\alpha} = \frac{1}{1-\left[\frac{\beta}{1+\beta}\right]} = (1+\beta).$$

→ The collector current is

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_0$$

$$\boxed{I_C = \beta I_B + (1+\beta) I_0}$$

→ The total Emitter current is

$$I_E = \frac{1}{1-\alpha}\left[I_B + I_0\right]$$

$$\boxed{I_E = (1+\beta)\left[I_B + I_0\right]}$$

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when I_0 - Neglected:

$$I_C = \alpha I_E$$

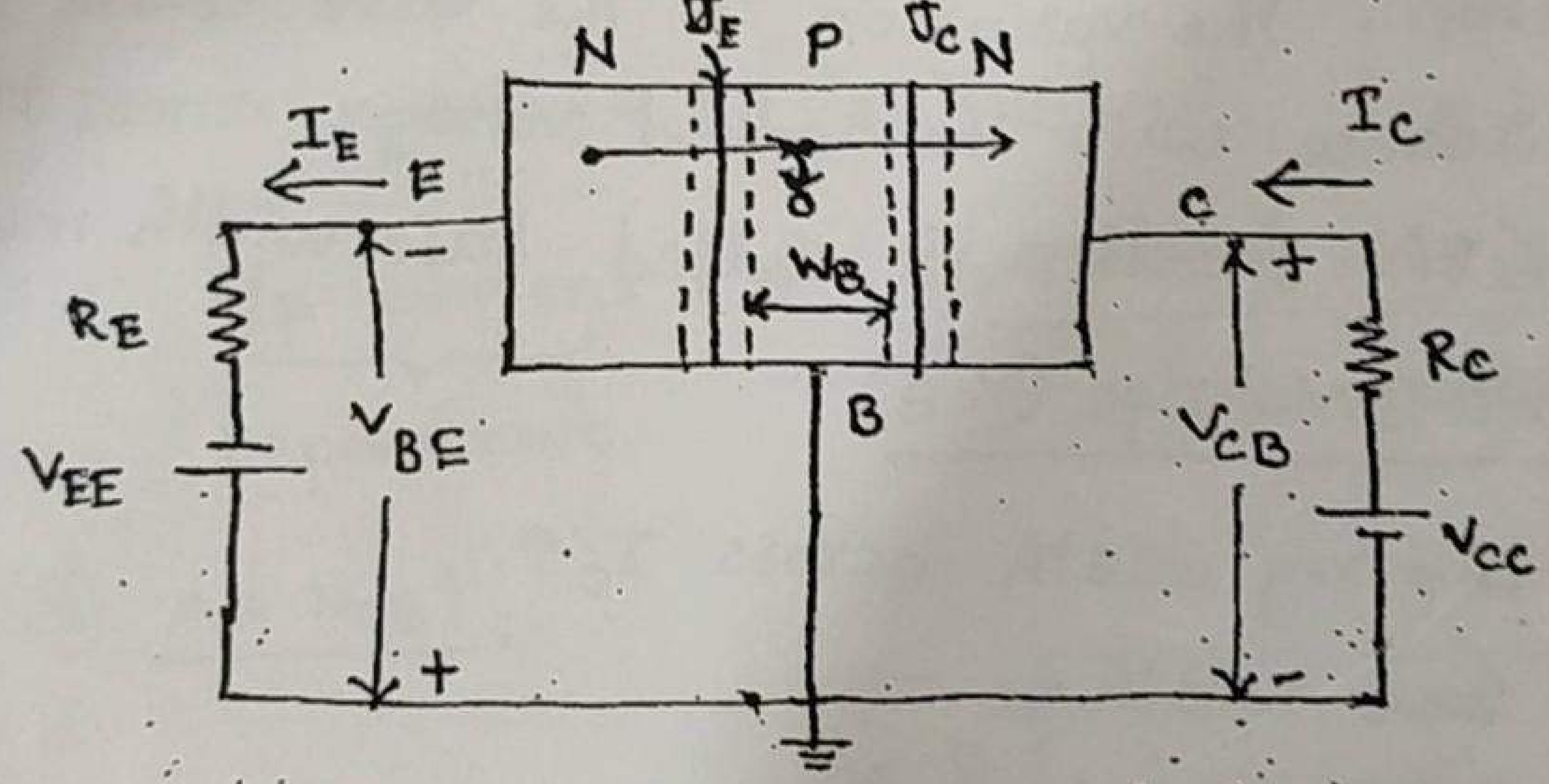
$$\boxed{I_C = \frac{\beta}{1+\beta} I_E}$$

$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B = \beta I_B}$$

$$\boxed{I_E = \frac{1}{1-\alpha} I_B = (1+\beta) I_B}$$

All the above equations valid for Active region of operation.

Base width Modulation :- (or) EARLY Effect :-



AS $V_{BE} \uparrow$

- Depletion region width across $J_E \downarrow$
- Base width $\uparrow$

$V_{BE} \uparrow\uparrow$ Base width $\uparrow\uparrow$

* when $V_{BE} = V_\gamma$. Depletion region width of J_E becomes zero.

AS $V_{BE} \uparrow$ (beyond V_γ) - There is no variation in Base width.

As $V_{CB}\uparrow$

- Depletion region width $\uparrow$

  (this $\uparrow$ more into lightly doped region i.e Base)

- Base width $\downarrow$

$V_{CB}\uparrow\uparrow$ Base width $\downarrow\downarrow$

At some particular voltage V_{CB}, the depletion region becomes max. & occupies the base region

Base width = 0.

The collector Junction permanently damages.

* The Base width modulation is related to the reverse bias voltage applied across the collector Junction. The variation of the base width in accordance with the applied voltage across the collector Junction is called base width modulation.

⇒ As R.B voltage (V_{CB}) $\uparrow$

- Dep. reg width across $I_C\uparrow$
- Base width $\downarrow$
- Temp across $J_C\uparrow$
- collector able to collect more no. of charged particles. $I_C\uparrow$
- Rate of recombination of $\bar{e}$ - holes pairs in the base $\downarrow$.

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Consequences of BWM :-

① As $V_{CB}\uparrow$

- Depletion reg. width across $J_C\uparrow$
- Base width $\downarrow$
- Recombination Rate in Base $\downarrow$
- $I_C\uparrow$

The value of 'I_c' depends on the value of V_{CB}

$$\underset{\Uparrow}{I_C} = f[\underset{\Uparrow}{V_{CB}}]$$

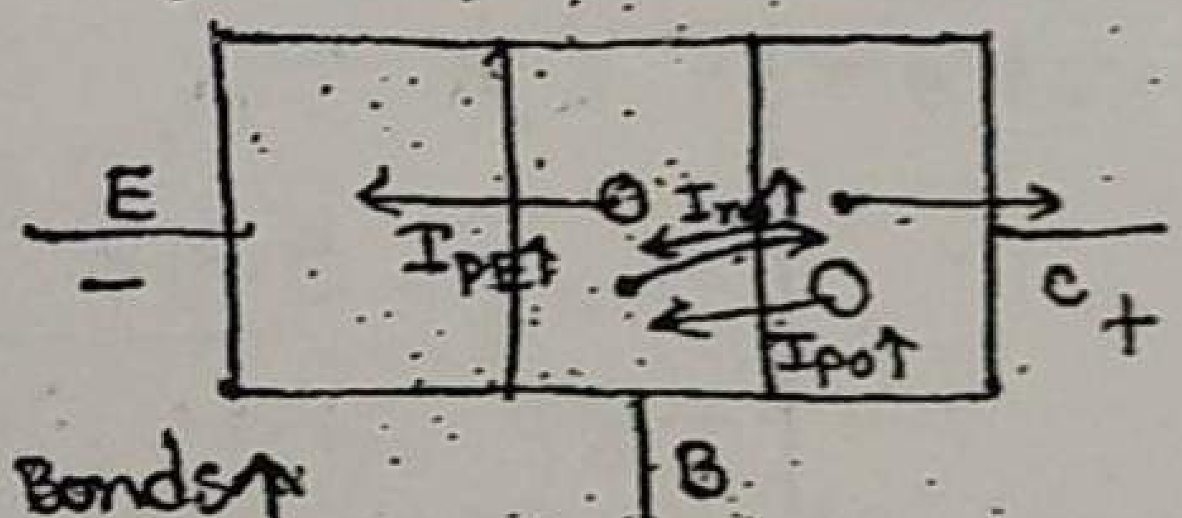
BJT is a current controlled Device.

$$I_c = f[I_E]$$

$$\therefore I_C = f[I_E, V_{CB}]$$

$$\underbrace{\text{o/p current}}_{\text{Dependent}} = f[\underbrace{\text{i/p current, o/p voltage}}_{\text{Independents.}}]$$

② As $V_{CB}\uparrow$:-



- Temp across in $J_C\uparrow$
- Breakage of covalent Bonds$\uparrow$ in C & B.
- e^- - hole pairs$\uparrow$ in C & B.
- $\underbrace{I_{no}\uparrow, I_{po}\uparrow}_{I_0\uparrow}$
- As $I_0\uparrow$ $I_C\uparrow$
- $I_{PE}\uparrow$ As $I_{PE}\uparrow$, $I_E\uparrow$

As $V_{CB} \uparrow - I_E \uparrow$

To maintain I_E at a constant level, $\downarrow V_{BE}$.

Dependingon the value of I_E $V_{BE} \downarrow$

By comparing V_{BE} & I_E $\Rightarrow$ $V_{BE} = f\,[I_E]$

By " V_{BE} & V_{CB} $\Rightarrow$ $V_{BE} = f\,[V_{CB}]$

$$\therefore V_{BE} = f\,[I_E, V_{CB}]$$

$$\boxed{\text{I/p voltage} = f\,[\text{i/p current, O/p voltage}]}$$

* **For a BJT transistor:-**

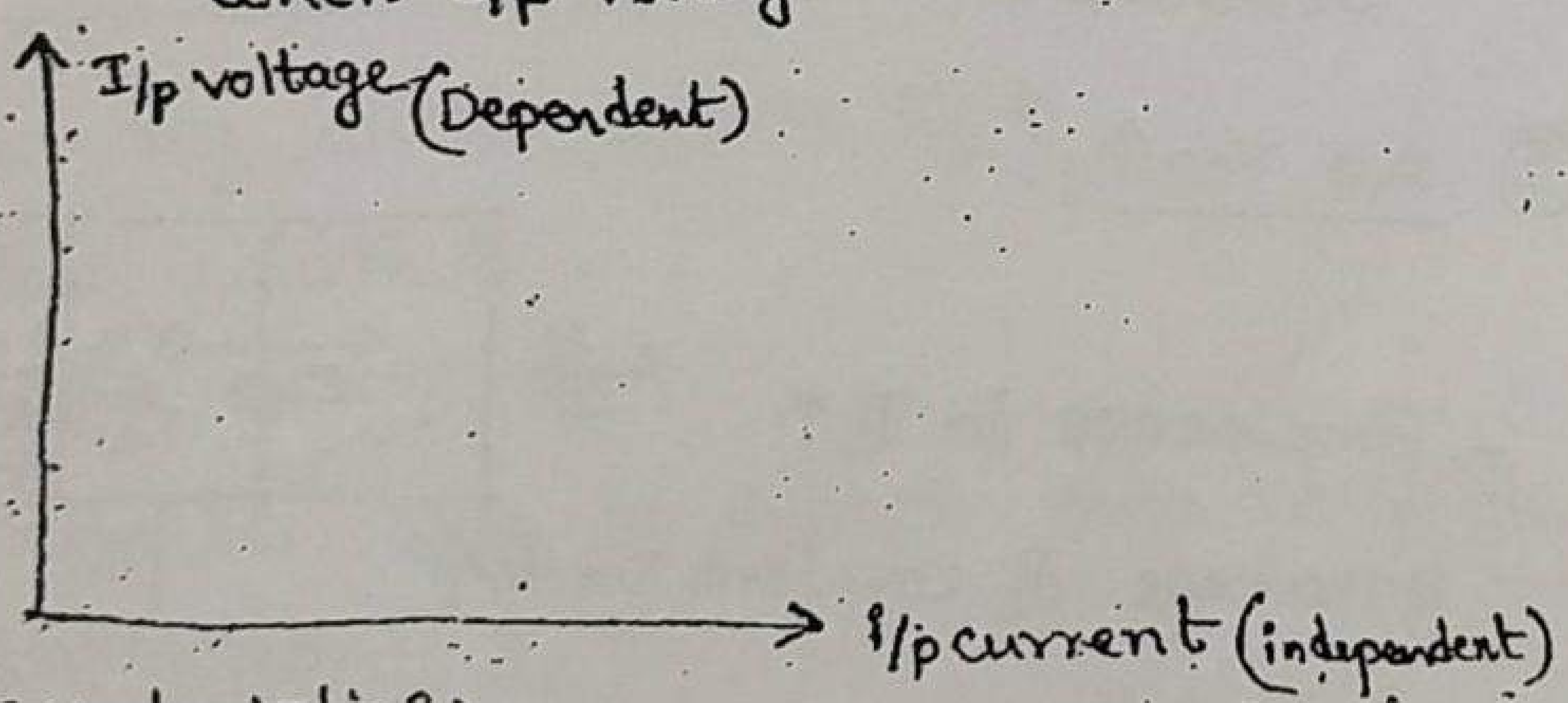
Independents (I/p current, O/p voltage)

Dependents (I/p voltage, O/p current)

I/p characteristics:-

I/p voltage V_s i/p current

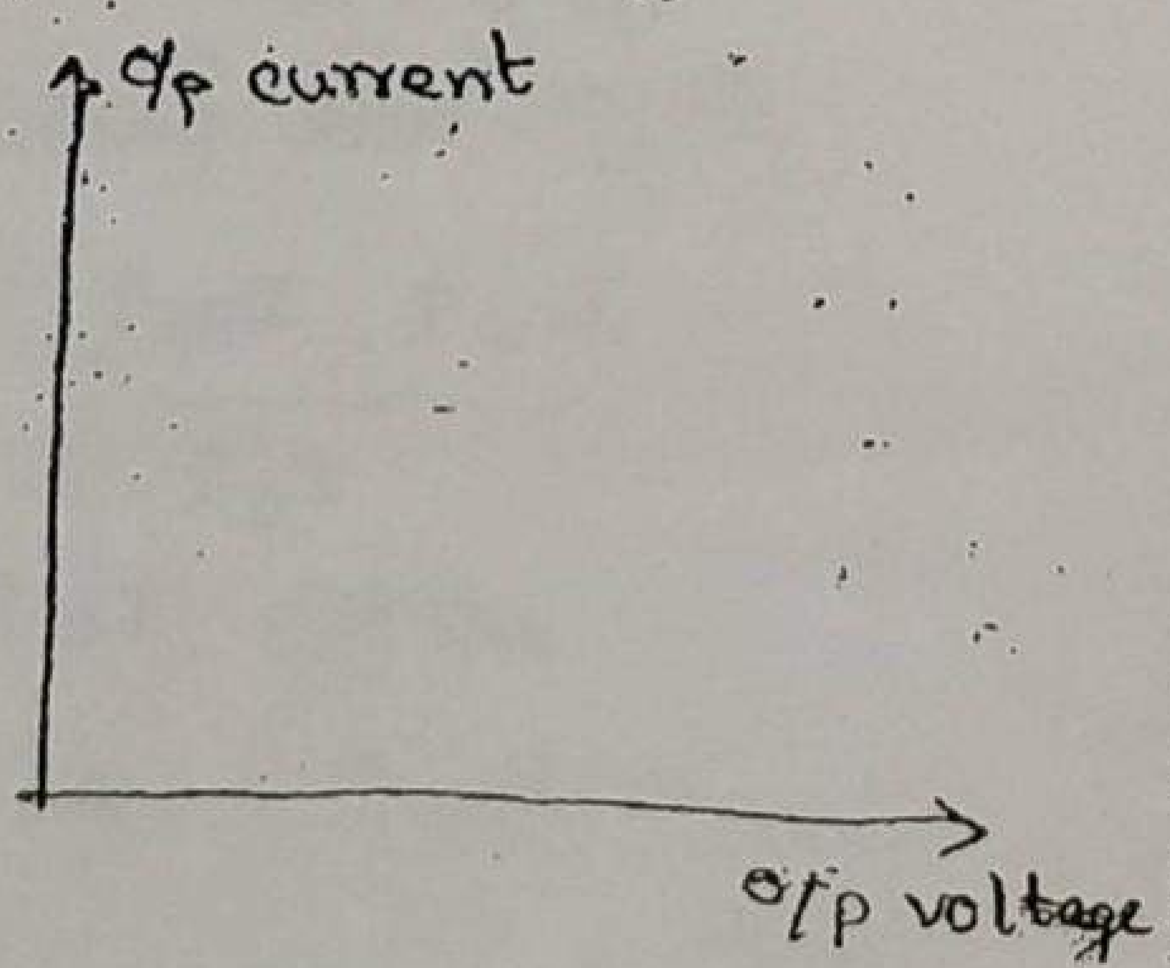
when O/p voltage = constant.



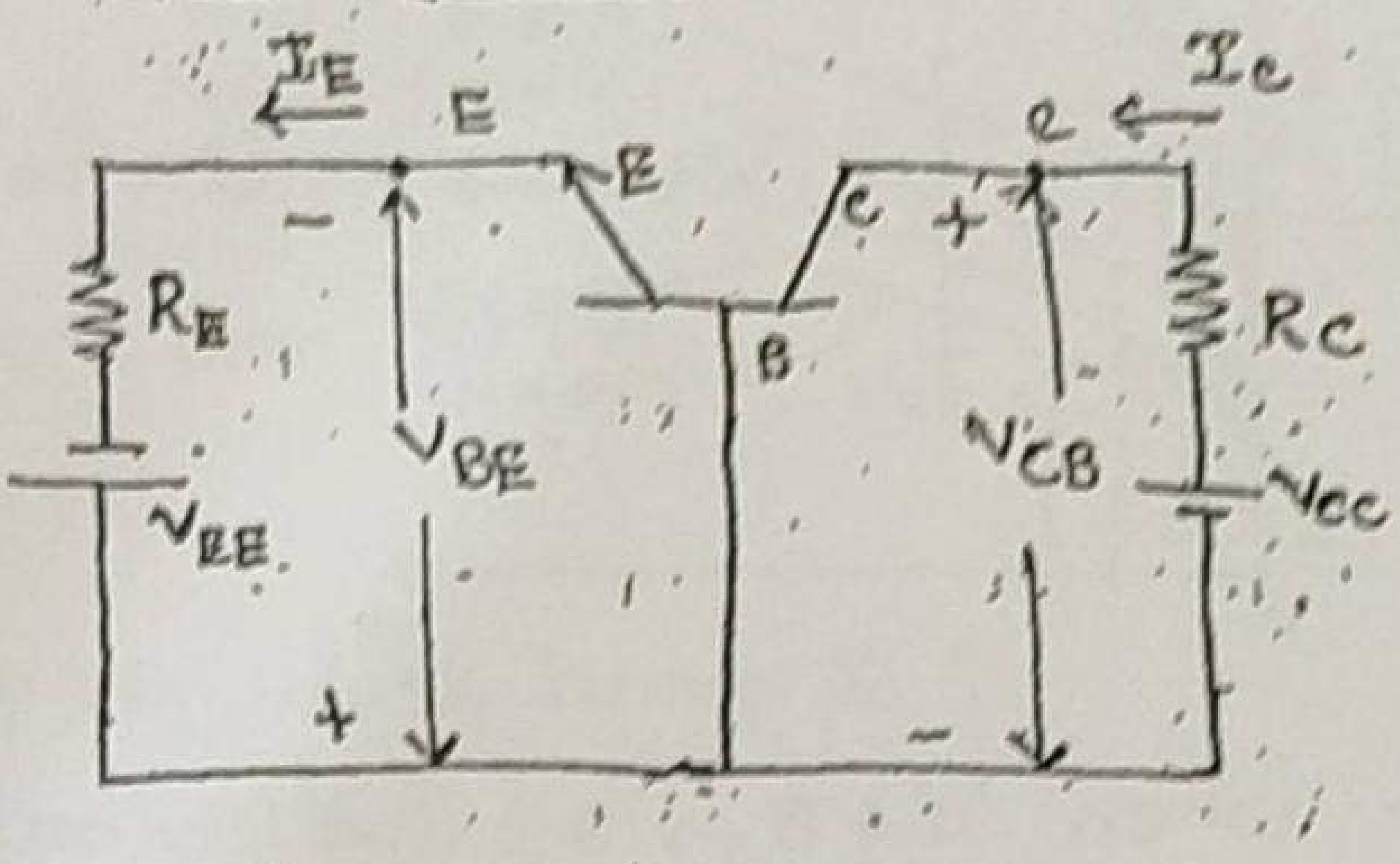
O/p characteristics:-

O/p current V_s O/p voltage

when i/p current = constant



Common Base characteristics :-



Inputs (V_{BE}, I_E)

o/p (V_{CB}, I_C)

For a BJT Transistor, Dependents (V_{BE}, I_C)
independents (I_E, V_{CB})

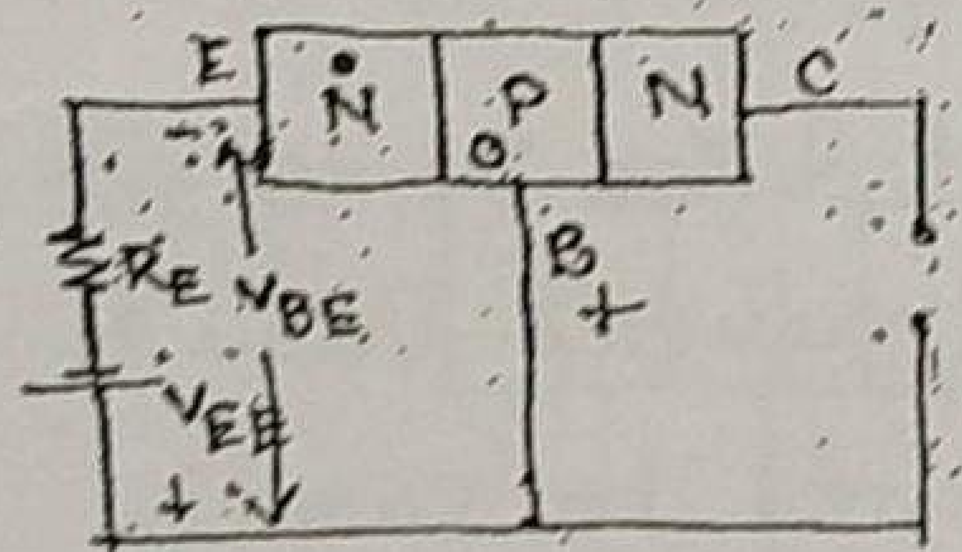
$$\therefore V_{BE} = f[I_E, V_{CB}] \rightarrow \text{i/p chara.}$$

$$I_C = f[I_E, V_{CB}] \rightarrow \text{o/p chara.}$$

Input characteristics :-

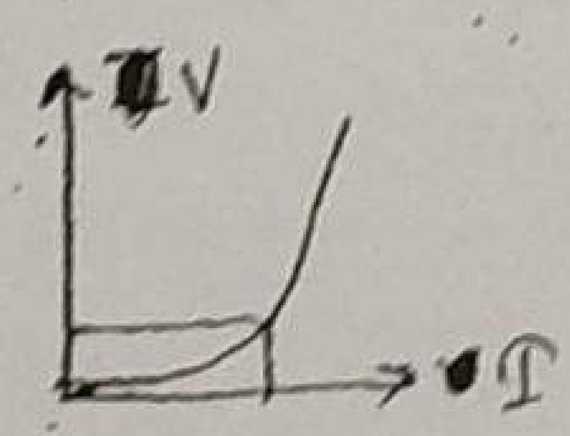
V_{BE} Vs I_E when $V_{CB} = \text{const.}$
- (i) C & B terminals O.C
- (ii) C & B " S.C i.e $V_{CB} = 0V$
- (iii) $V_{CB} \neq 0V$.

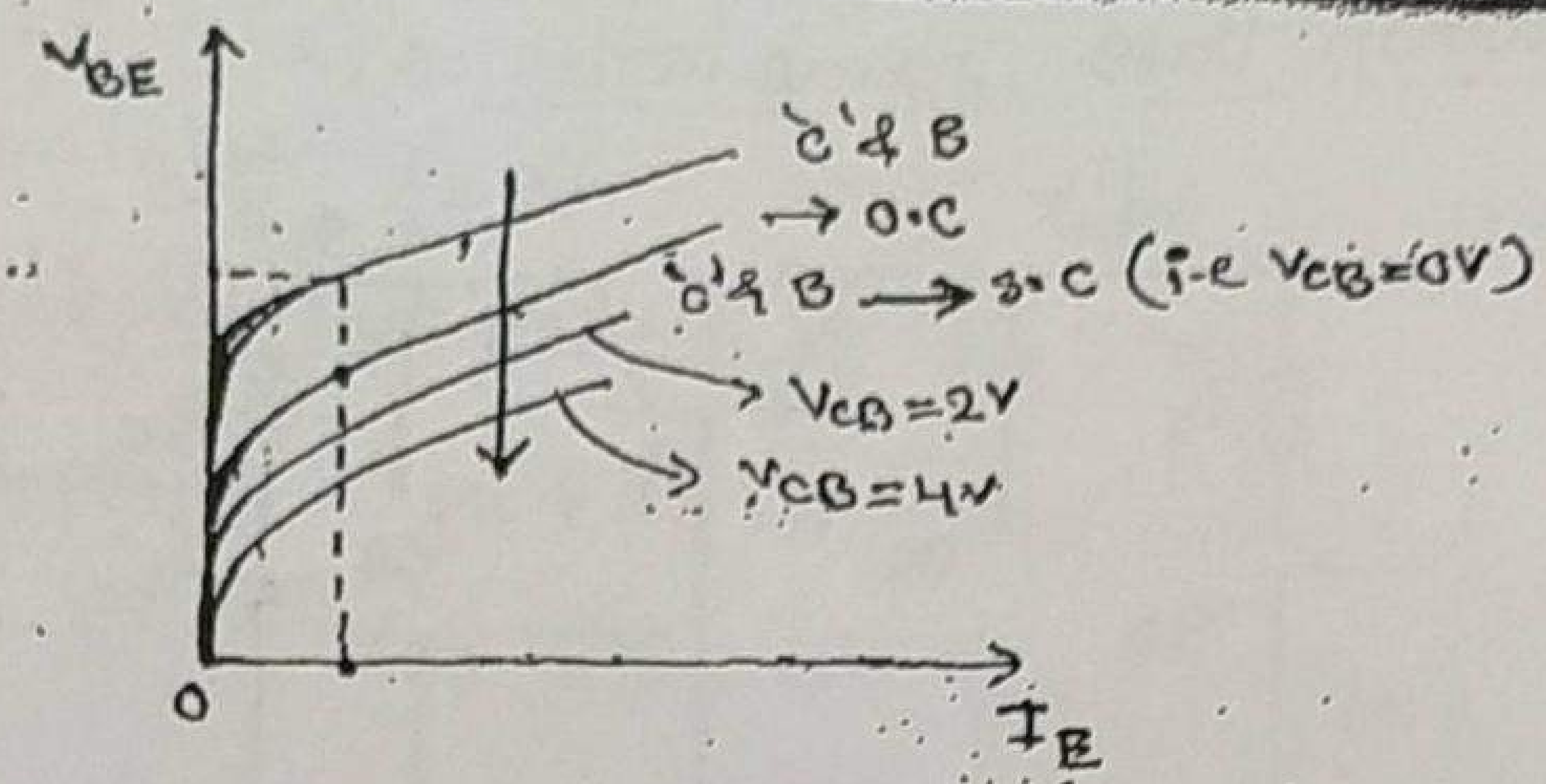
Case (i) when C & B → O.C



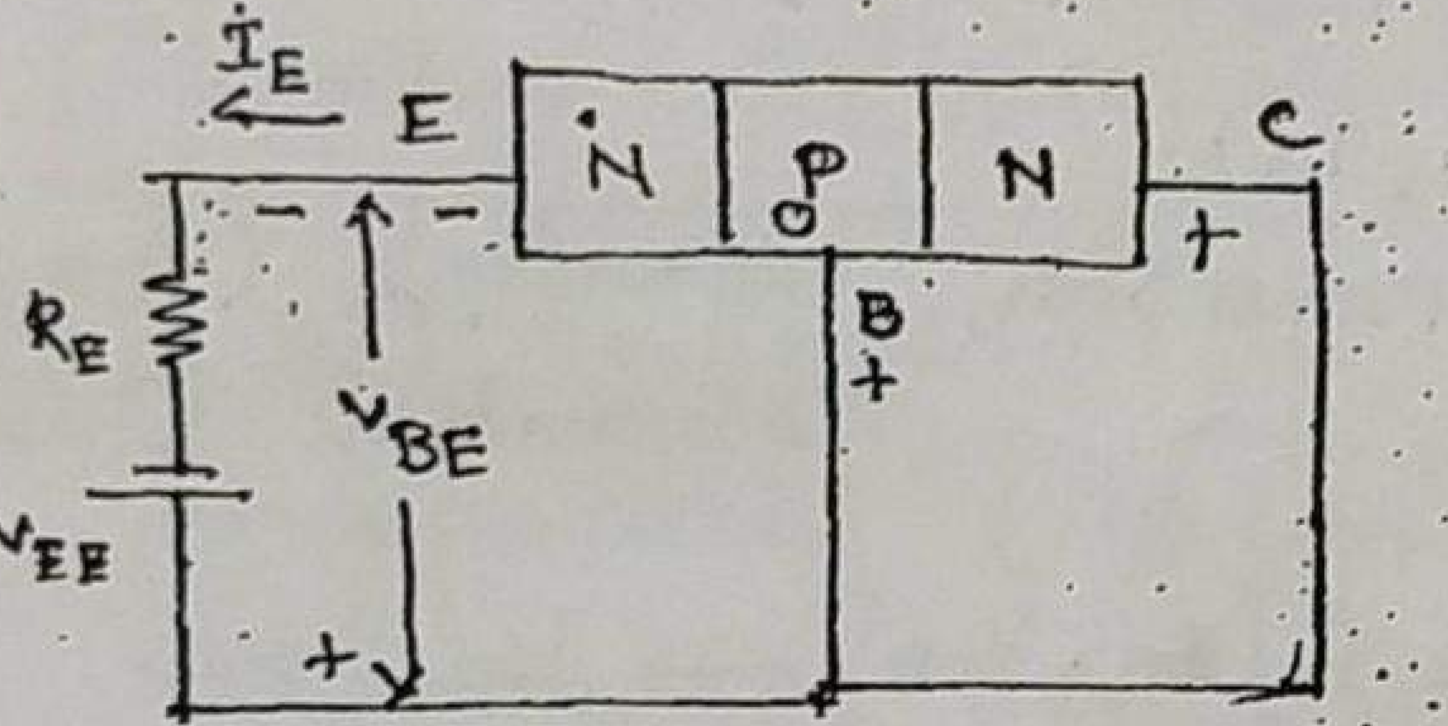
The chara. of the transistor in this case is similar to the char. of a F.B PN Junction diode. with axes interchanged

diode cha





case (ii):- when 'C' & B → S.C i.e $\underline{V_{CB}=0V}$



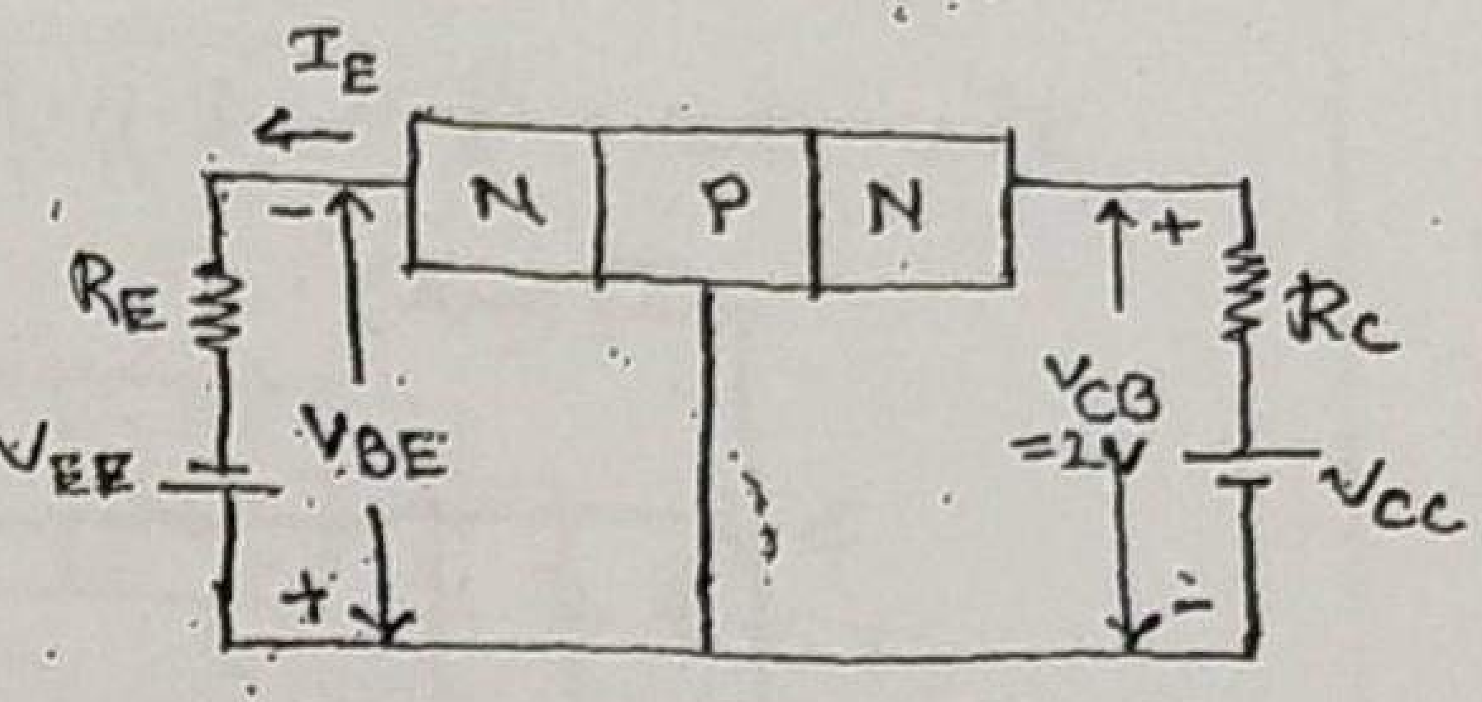
- The C & B are at same potential.
- The 'C' & 'B' potentials ~~repels~~ repels the holes present in Base.
- The no.of holes crossing $J_E \uparrow$ ($I_{PE} \uparrow$)
- The 'C' & 'B' potentials able to attract the $\bar{e}$ from 'E': so the no.of $\bar{e}$ crossing.

$$J_E \uparrow \quad (I_{NE} \uparrow)$$
$$I_E \uparrow$$

- I_E is more in this case compared to case(i)
- To maintain I_E as constant $\downarrow V_{BE}$ i.e to get a particular value of I_E the required Value of V_{BE} is LESS in this case compared to case(i).

Case(iii):- when $V_{CB} \neq 0V$

Let $V_{CB} = 2V$.



* As V_{CB} ↑ from 0 to 2V

As V_{CB} ↑

- Dep reg. width across J_C ↑
- Base width ↓
- Recombination rate in Base ↓
- Temp across J_C ↑
- Breakage of covalent bonds in 'C' & B ↑
- I_{no} ↑, I_{po} ↑, I_{pE} ↑,

As I_{pE} ↑ → I_E ↑

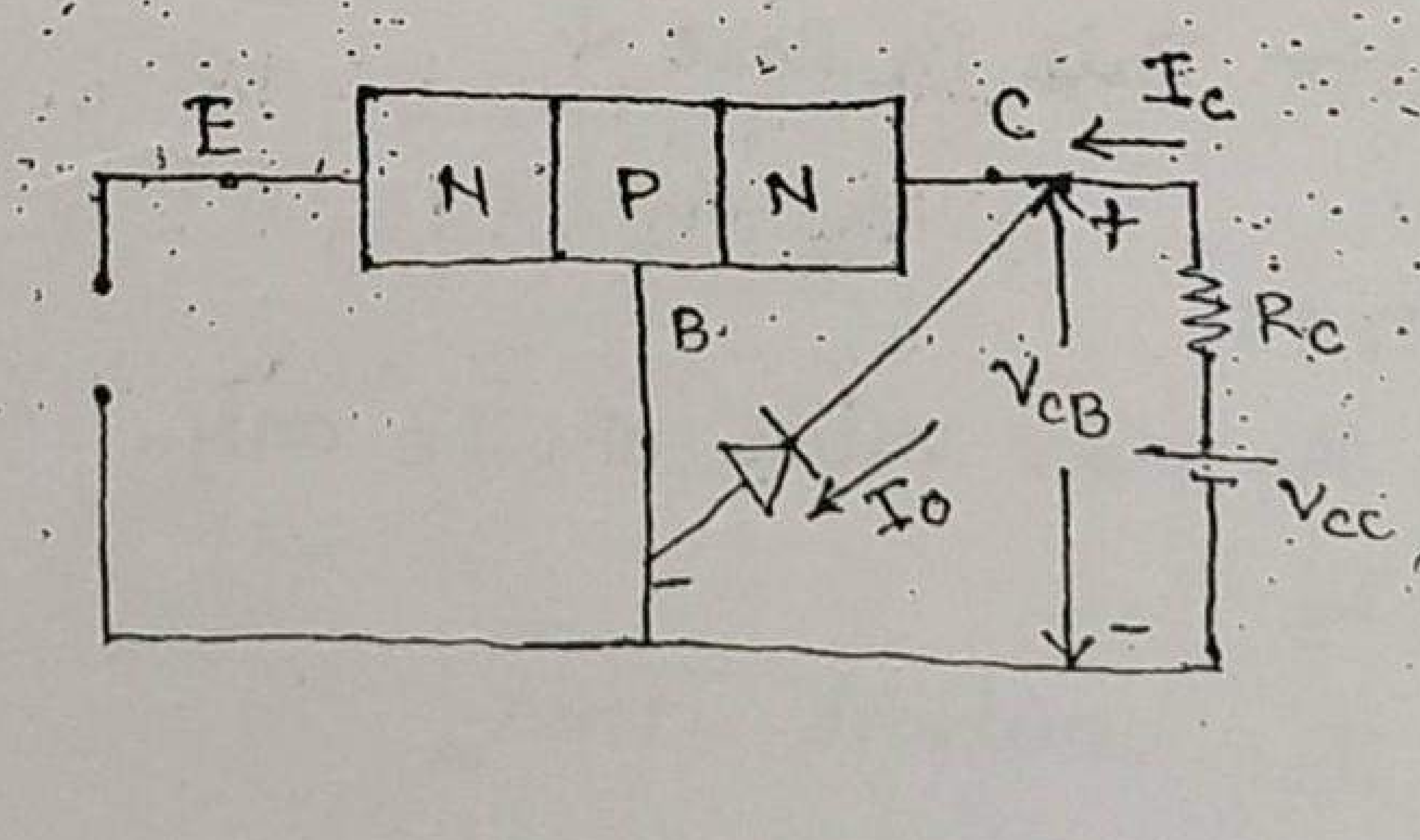
- This current is more than case (ii)
- To maintain I_E as const: ↓ V_{BE} i.e To get a particular value of I_E the req value of V_{BE} is less in this case compared to case (ii).

Output characteristics:-

I_C vs V_{CB} when I_E = const $\begin{cases} \text{(i) } I_E = 0 \\ \text{(ii) } I_E \neq 0 \end{cases}$

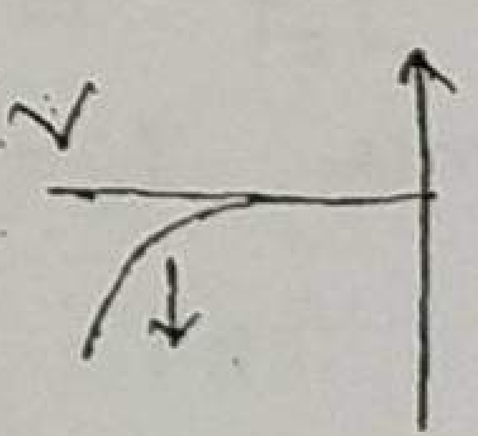
Case(i) when $I_E = 0$

i.e B & E terminals O.C

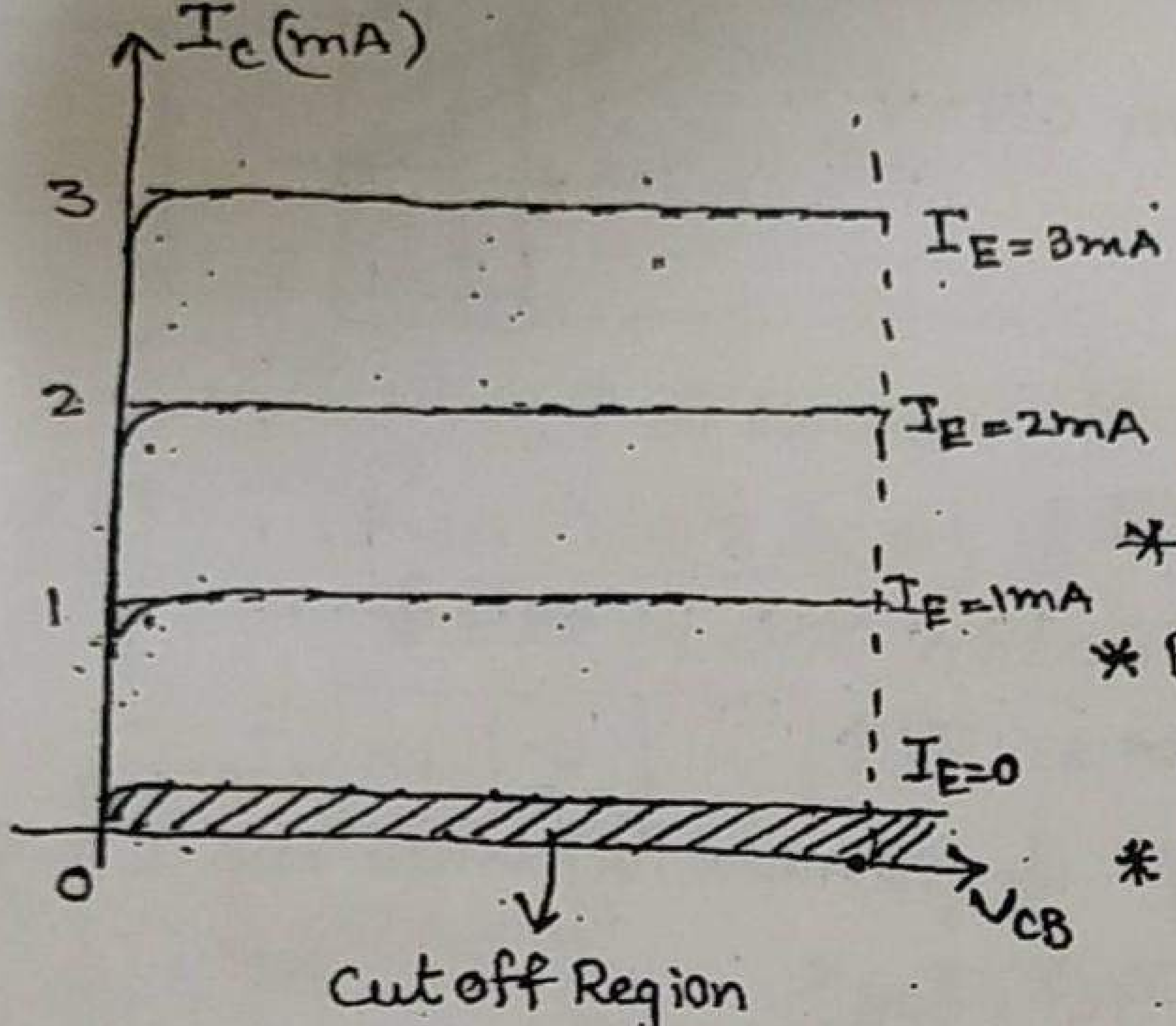


$I_C = I_0 = I_{CBO}$

E' - O.C



The char. of the transistor in this case is similar to the char. of a R.B. PN-Junction diode.



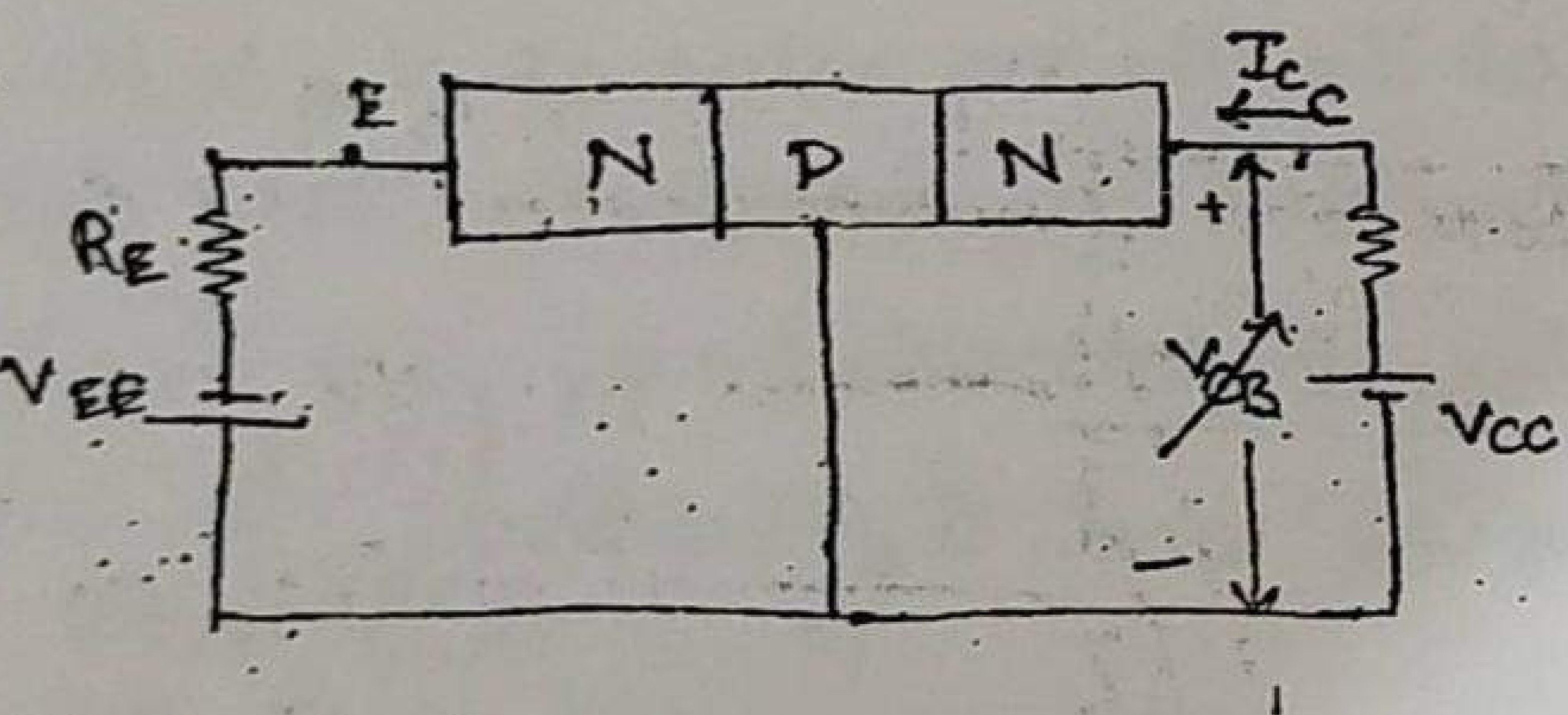
	Ge	Si
T = 27°C	1μA	1nA
47°C	4μA	4nA

* As V_{CB} ↑ Temp across J_C ↑
* Breakage of covalent bonds ↑ in 'C' & Base.
* I_{no} ↑ I_{po} ↑ = I_0 ↑ I_C ↑

As V_{CB} ↑ I_C ↑

<u>case (ii)</u>: when $I_E \neq 0$.

· Let $I_E = 1mA$ (constant)



As V_{CB} ↑

- Depletion region width ↑ , Base width ↓
- Recombination Rate in Base ↓
- I_C ↑

As V_{CB} ↑↑ I_C ↑↑

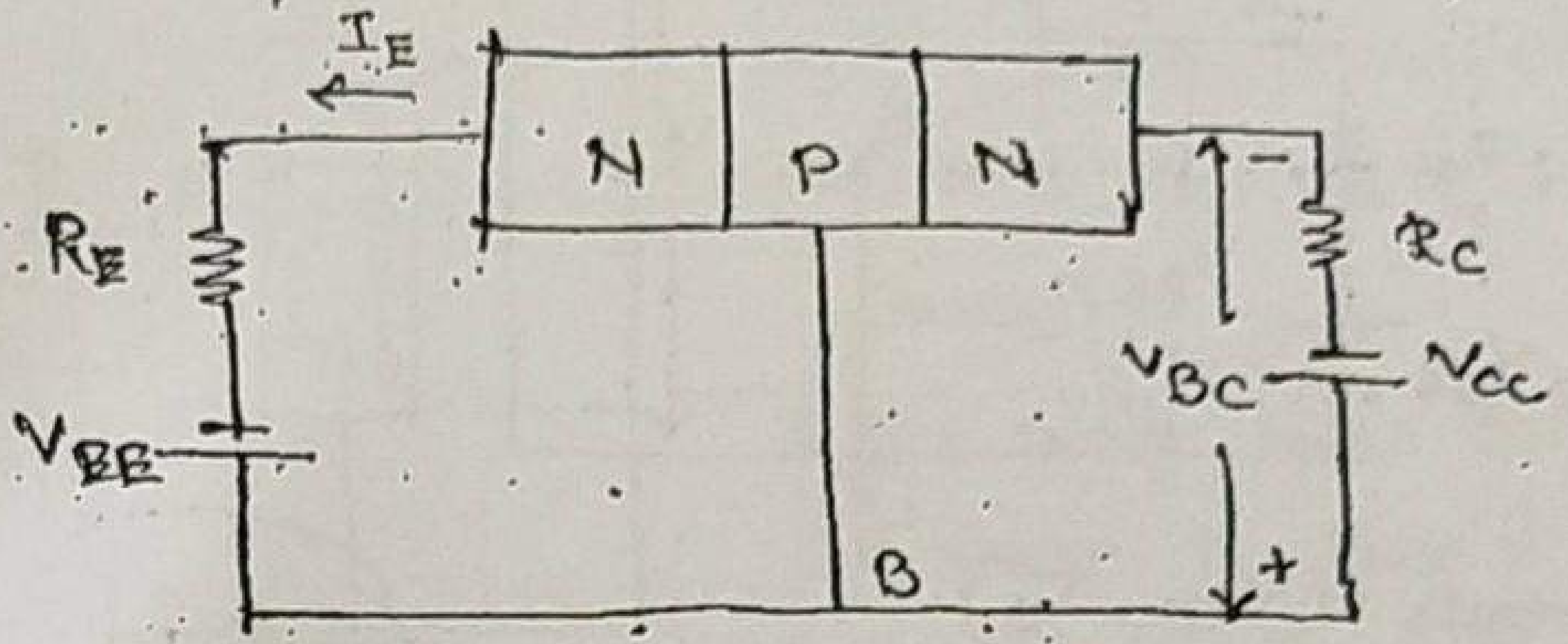
I_C ↑ to the max value of I_E only.

once $I_C = I_E$

V_{CB} ↑ I_C = constant = 1mA.

Case (iii) For Saturation Region :-

J_E - F.B & J_C - F.B



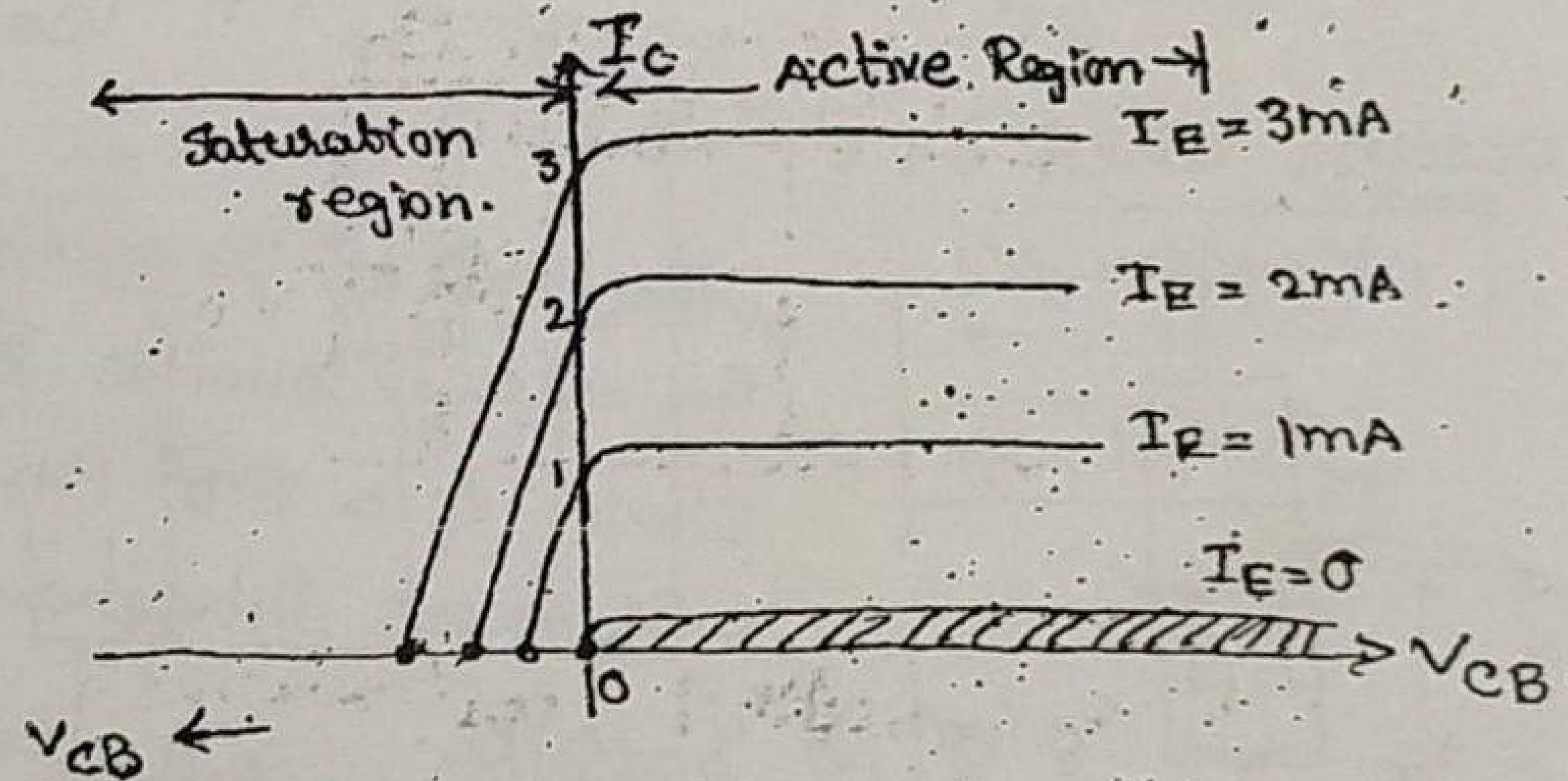
when $I_E = 1mA$ (constant)

As $V_{BC}\uparrow$ - 'c' repels the $\bar{e}$ $I_C \downarrow$

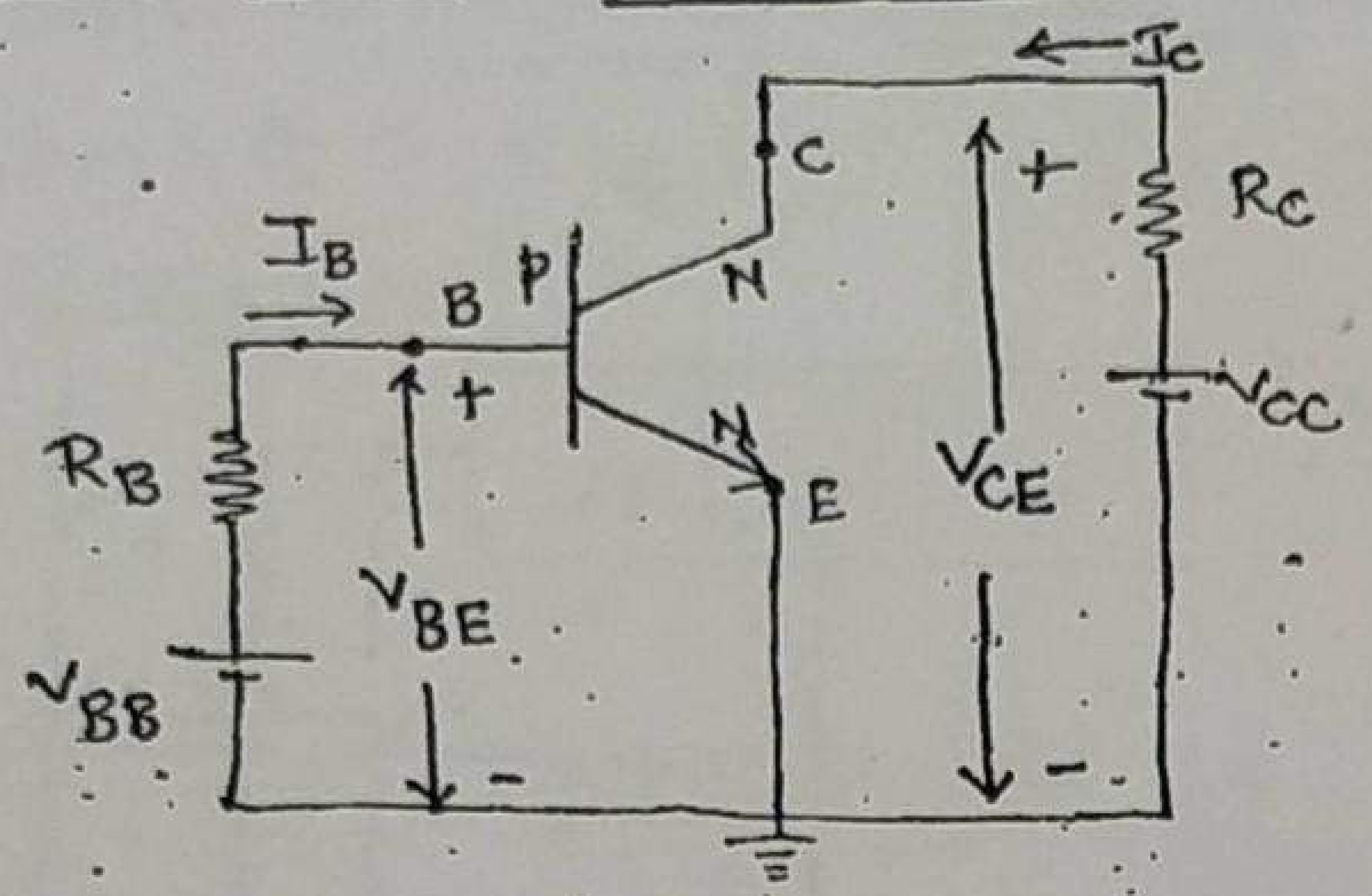
$V_{BC}\uparrow\uparrow$, $I_C\downarrow\downarrow$

At some particular voltage no. of charged particles collected by 'c'.

from E becomes zero.



Common Emitter characteristics :-



$V_{CC} >> V_{BB}$

Inputs (V_{BE}, I_B)

o/p (V_{CE}, I_c)

For a BJT Transistor

Dependents (V_{BE}, I_c)

Independents (V_{CE}, I_B)

i/p char.

$V_{BE} = f[I_B, V_{CE}]$

$I_c = f[I_B, V_{CE}]$

o/p char.

Input characteristics :-

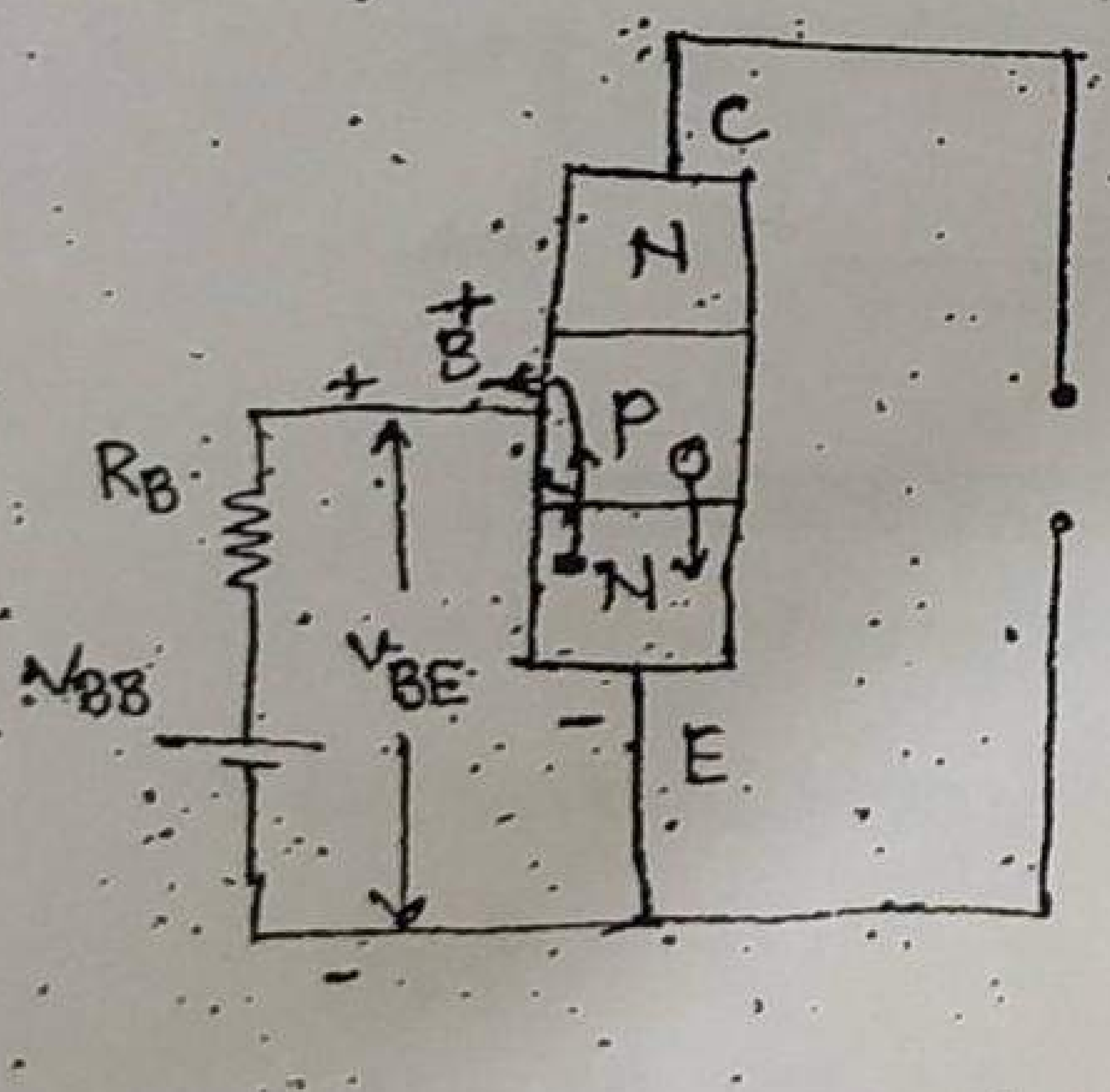
V_{BE} vs I_B when V_{CE} = const

(i) C & E → O.C

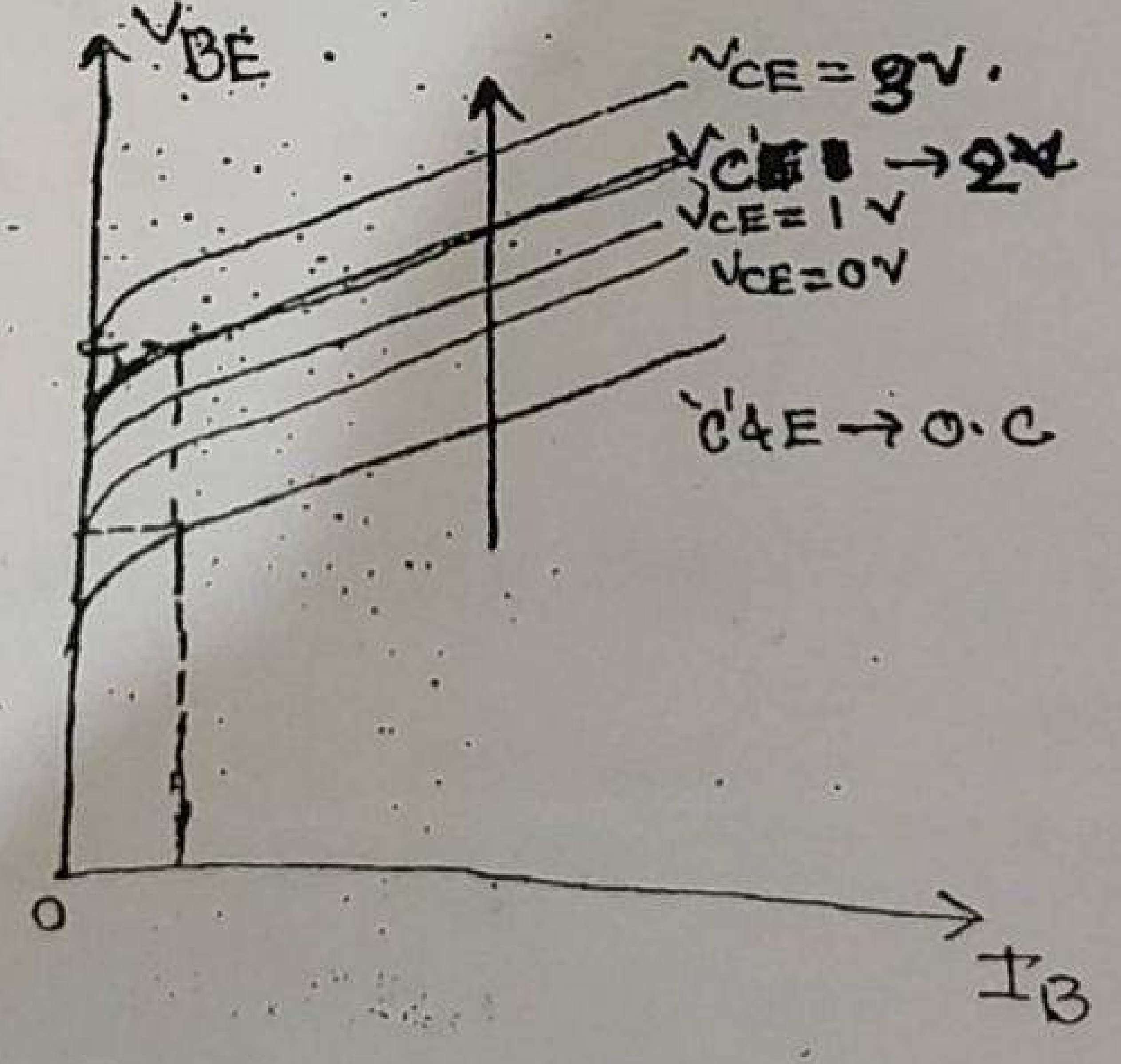
(ii) C & E → S.C i.e $V_{CE} = 0V$

(iii) $V_{CE} \neq 0V$.

Case(i) :- when C & E → O.C

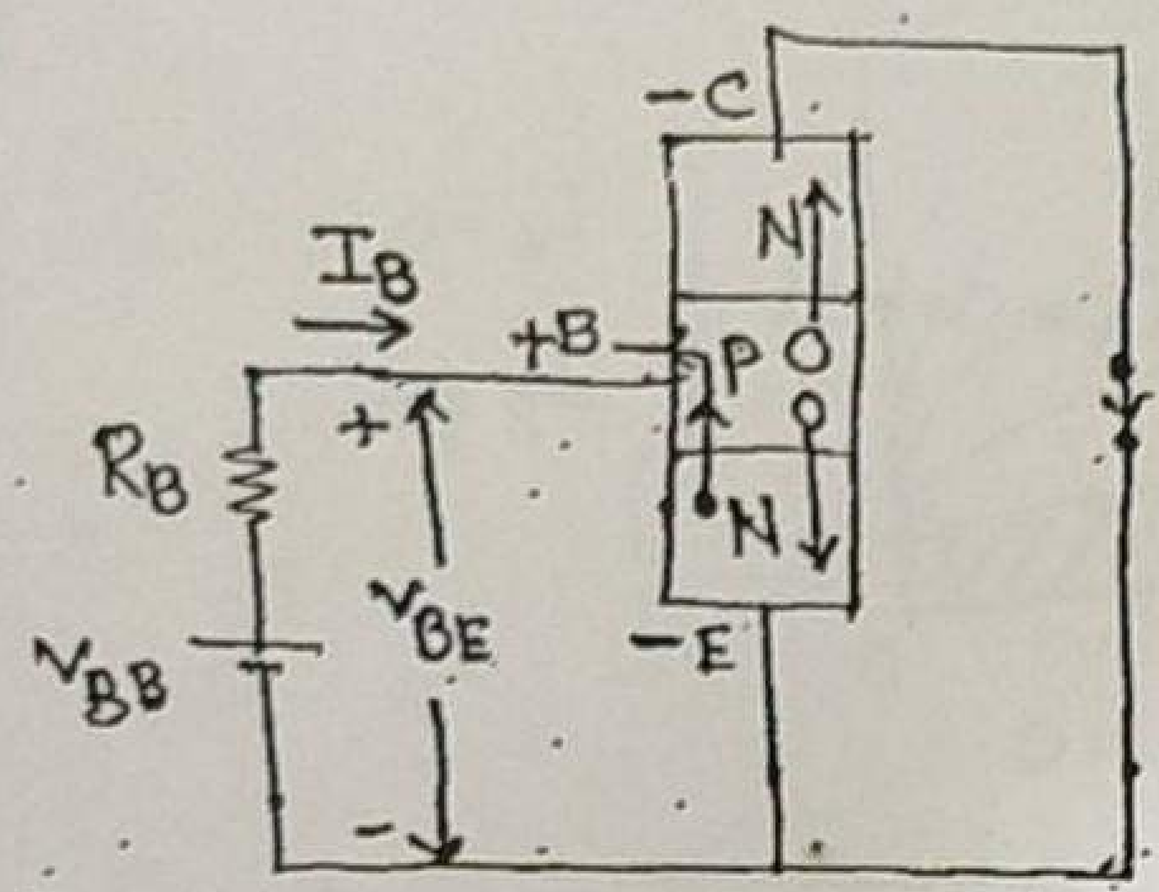


The char. of the transistor in this case is similar to the char. of a F.B PN jn diode with axes interchanged.



Case (ii) when 'c' & E → S.C

$V_{CE} = 0V$



* All the maj. carriers of 'E' collected by 'B'. There is no change in current due to $\bar{e}$ b/w 'B' & 'E' in case (i) & case (ii)

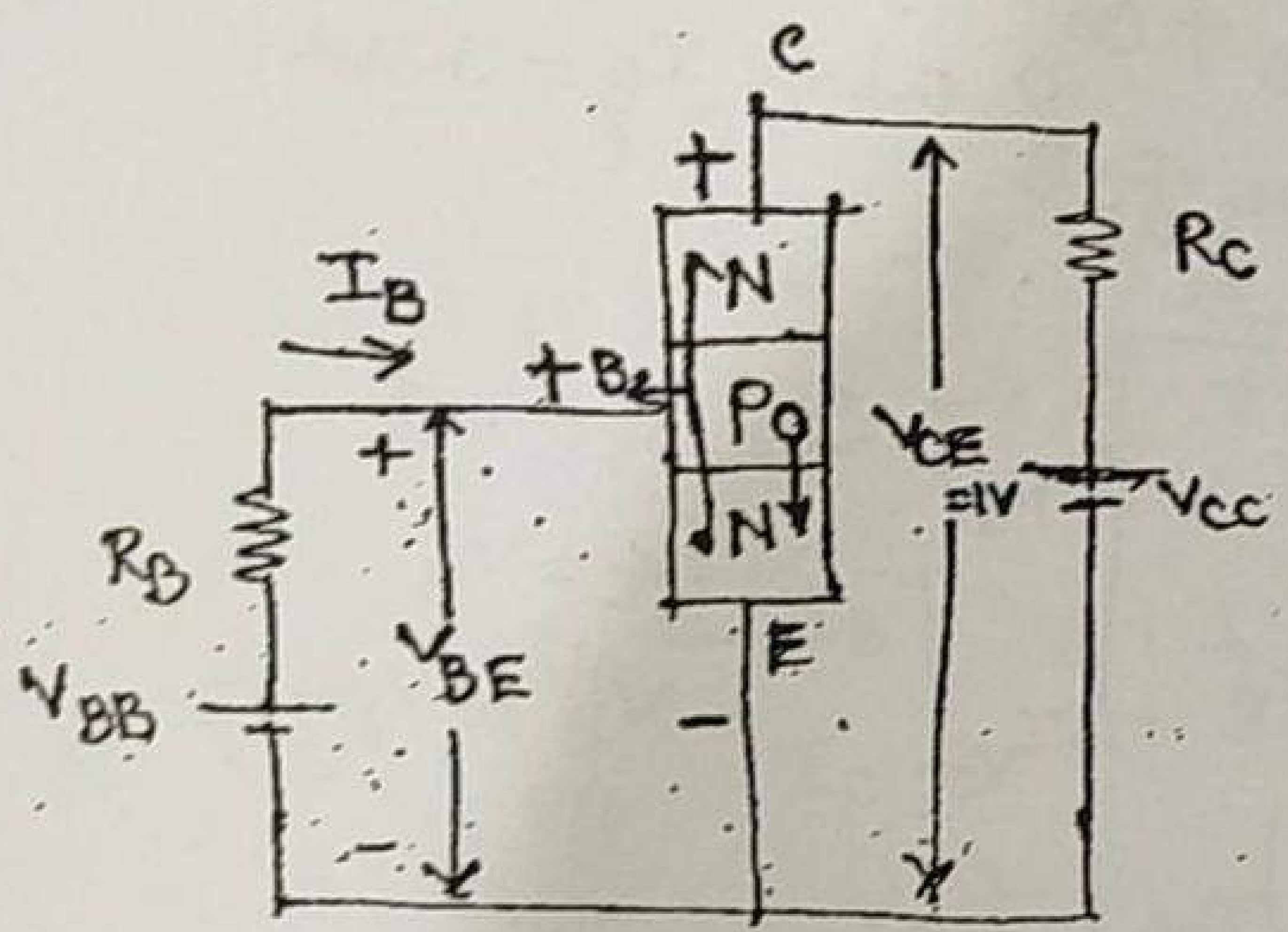
* The no. of holes collected by the 'E' from the Base ↓

∴ The hole current b/w 'B' & E = ↓

* To maintain I_B as const. increases the V_{BE} value.

i.e to get a particular value of I_B the req. value of V_{BE} is More in this case compared to case (i).

Case (iii) when $V_{CE} \neq 0$ Let $V_{CE} = 1V$.



$V_{BE} = V_\gamma$

$V_B - V_E = V_\gamma$

$\boxed{V_B = V_\gamma + V_E}$

$\boxed{V_C = 1 + V_E}$

$V_C > V_B$

* The no. of $\bar{e}$'s collected by 'B' from 'E' ↓

The $\bar{e}$ current b/w 'B' & 'E' ↓

The no. of holes collected by 'E' from B ↑.

The hole current b/w 'B' & 'E' ↑

∴ The resultant current 'B' & E ↓, I_B ↓

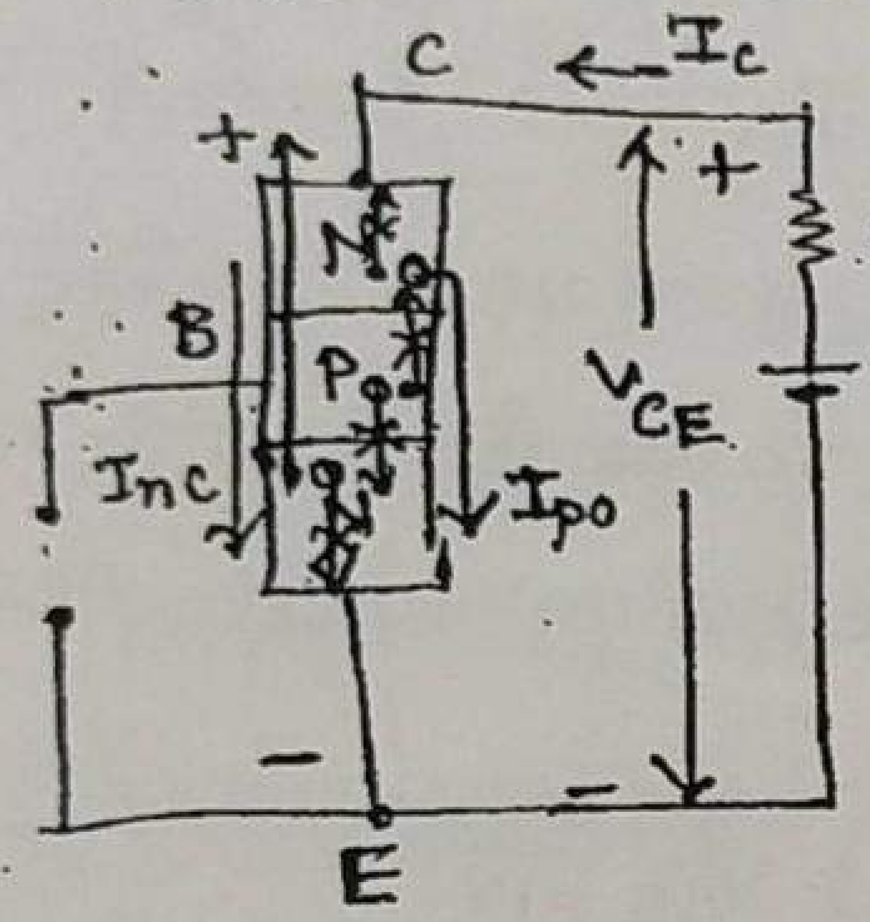
To maintain I_B as constant ↑V_{BE} i.e to get a particular value of I_B the required value of V_{BE} is more in this case compared to case (ii).

output characteristics:-

$$I_C \text{ vs } V_{CE} \text{ when } I_B = \text{const} \begin{cases} I_B = 0 \\ I_B \neq 0 \end{cases}$$

Case (i):- when $I_B = 0$

→ B & E terminals are O.C

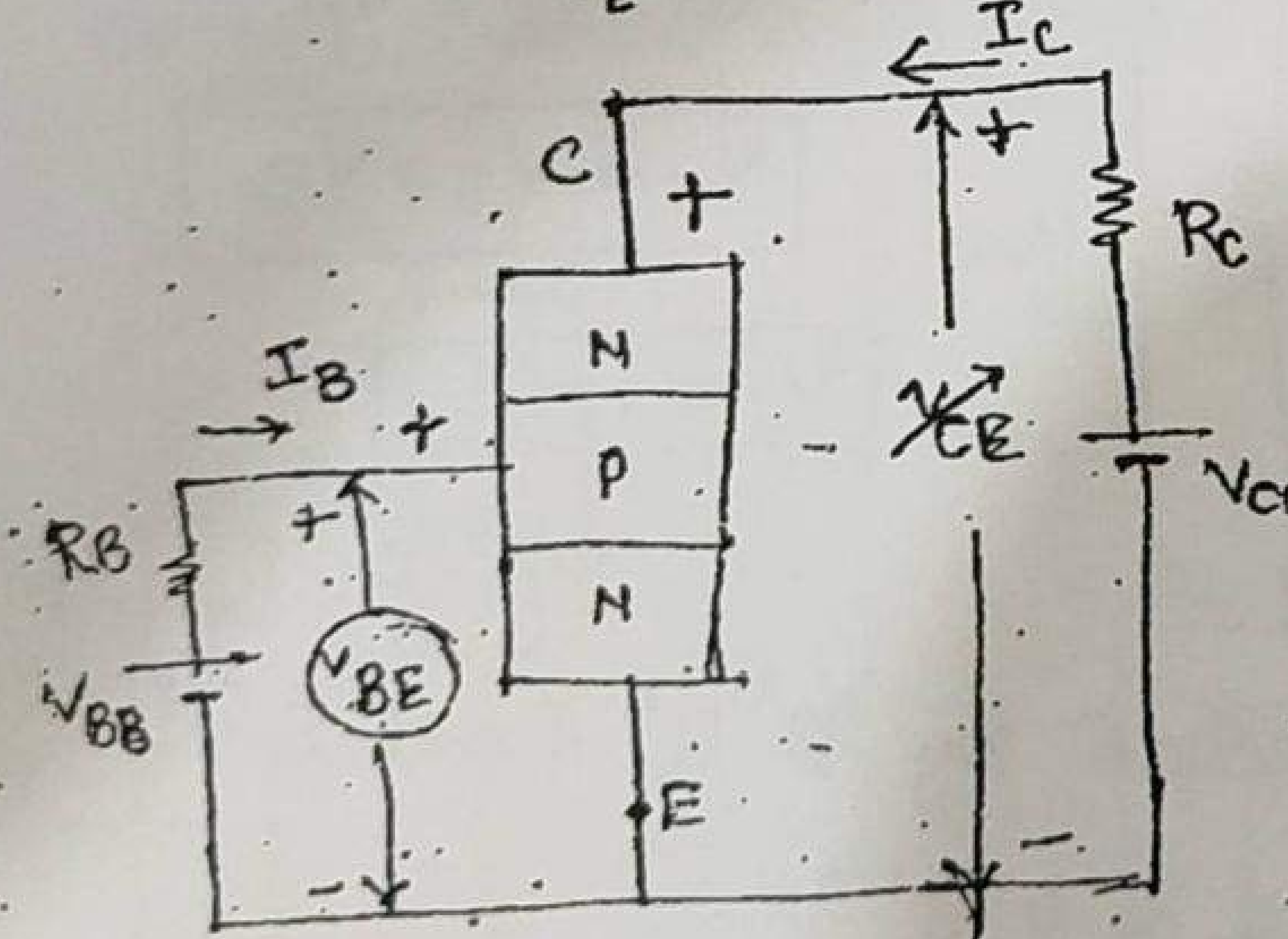


$\boxed{I_C = I_{nc} + I_{po}}$

As $V_{CE} \uparrow$ $I_C \uparrow$

case (ii):- when $I_B \neq 0$ Let $I_B = 5\mu A$.

'J_E' must be F.B



$V_{CE} = 0$

$V_C \doteq V_E$

$V_B = V_\gamma + V_E$.

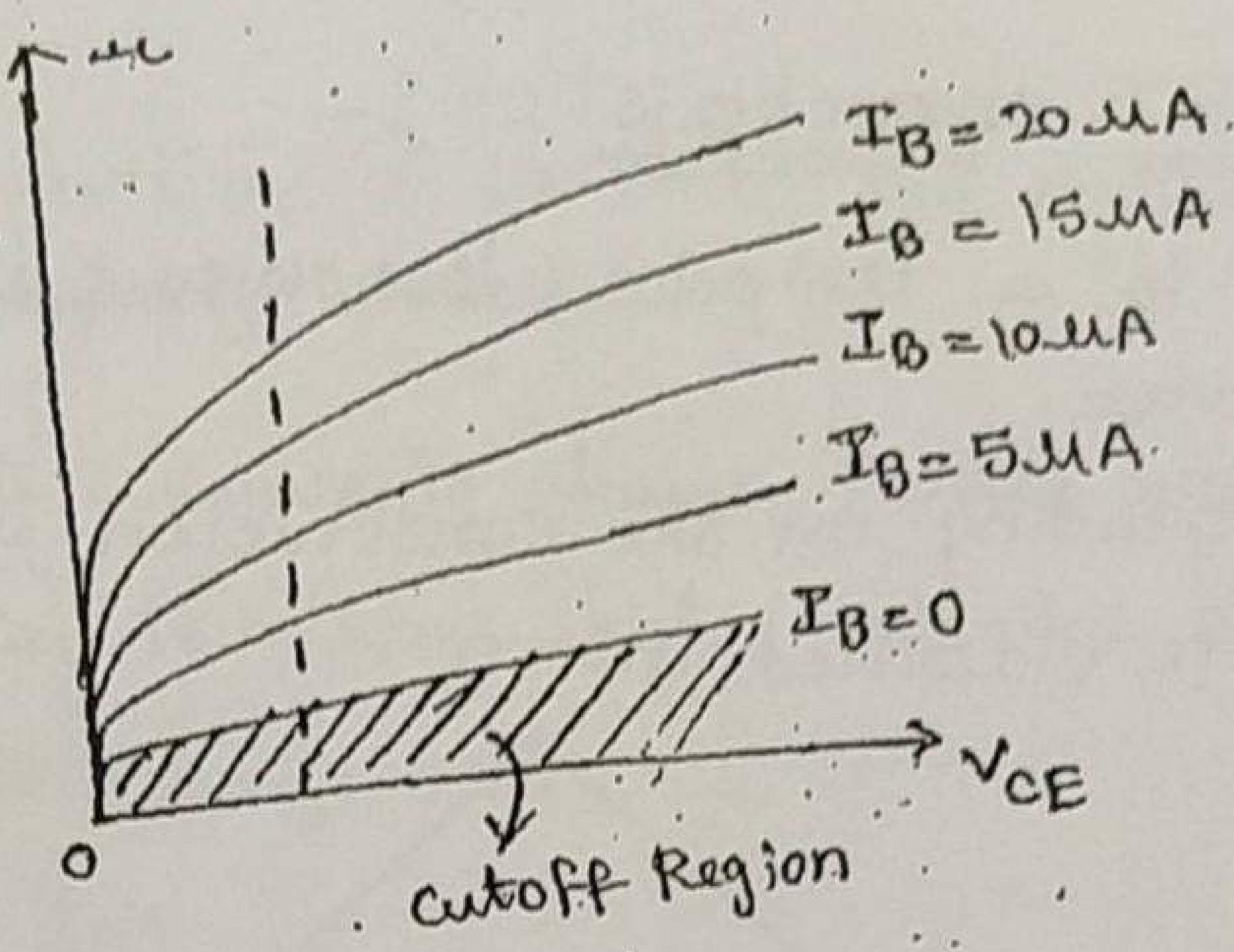
As $V_{CE} \uparrow$

(i) when $V_{CE} < V_{BE} \Rightarrow J_C \to F.B$

→ saturation Region.

(ii) when $V_{CE} > V_{BE} \Rightarrow J_C \to R.B$

→ Active Region.



* The common collector characteristics are similar to common emitter characteristics. In i/p characteristics I_C replaced V_{BE} replaced by V_{CB}. In o/p characteristics I_C replaced by I_E.

* The phase shift b/w i/p & o/p for

(i) CB → 0°
(ii) CE → 180°
(iii) CC → 0°.

* CB $\begin{cases} i/p - I_E \\ o/p - I_C \end{cases}$ ⇒ $+I_C = +I_E - I_B$ 0°

* CE $\begin{cases} i/p \rightarrow I_B \\ o/p \rightarrow I_C \end{cases}$ $+I_C = +I_E - I_B$ 180°

* CC $\begin{cases} i/p \rightarrow I_B \\ o/p \rightarrow I_E \end{cases}$ $+I_E = +I_C + I_B$ 0°

FET characteristics :-

FET is a unipolar, low Noise & voltage controlled Device.

* Depending on the construction principle the FETS are classified into

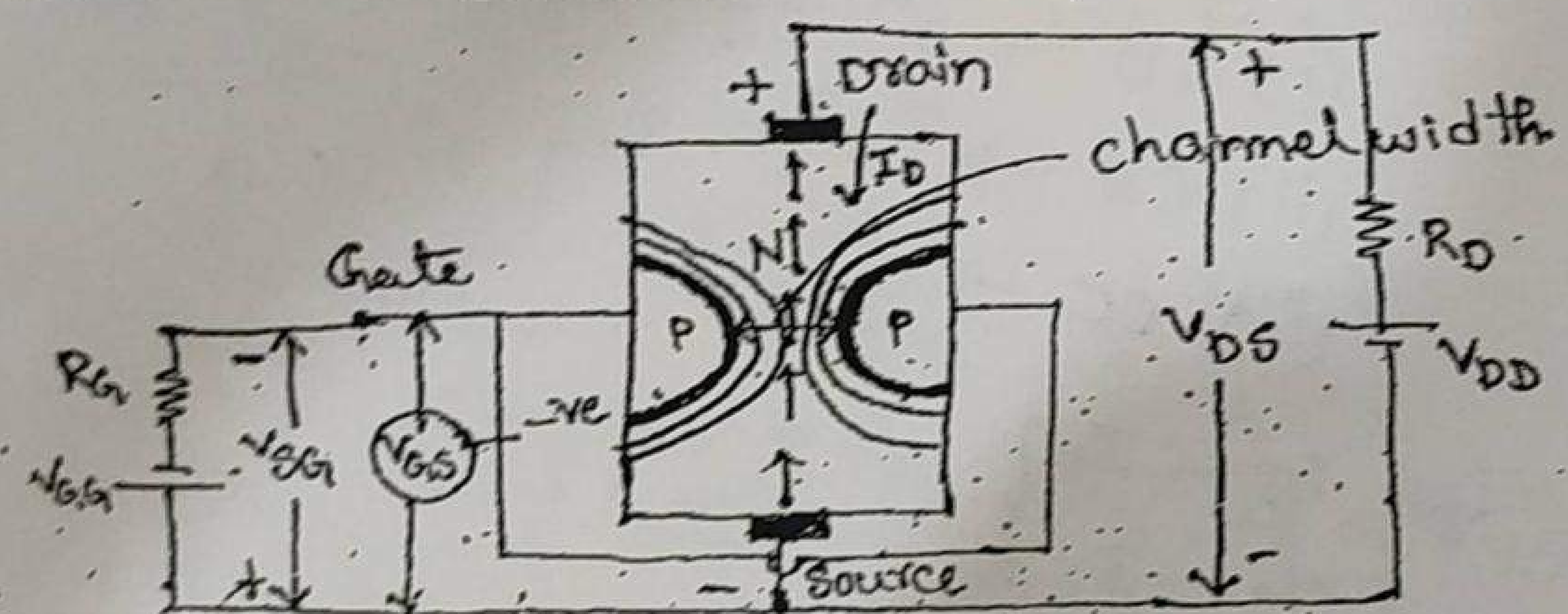
Junction FET (JFET)

MOSFET (or) IGFET

D-MOSFET

E-MOSFET

JFET :- construction of N-channel JFET :-



first select the N type bar whose resistance is exactly divided 2 heavily doped p-type semiconductor are exactly diffused into N-type silicon bar.

The gap b/w two depletion regions are called channel width.

JFET have 3 terminals source, Drain, gate.

To make conduction of current the N-channel JFET must be properly biased.

i.e

1. Gate - source is always Reverse biased.

2. Drain is always higher potential than source.

V_{DS} is always +ve

As $V_{DS}\uparrow$ $I_D\uparrow$

$V_{DS}\uparrow\uparrow$ $I_D\uparrow\uparrow$

* I_D value depends on V_{DS}. $\boxed{I_D = f[V_{DS}]}$

→ V_{GS} is always Negative values.

As $V_{GS}\uparrow$ - Depletion region widths $\uparrow$, channel width $\downarrow$

$I_D\downarrow$

As $V_{GS}\uparrow\uparrow$ $I_D\downarrow\downarrow$ $\boxed{I_D = f[V_{GS}]}$

$I_D = f[V_{GS}, V_{DS}]$

→ Voltage controlled Device.

$I_D = f[V_{GS}, V_{DS}]$

I_D vs V_{DS} when $V_{GS} = \text{const}$

- Drain characteristics

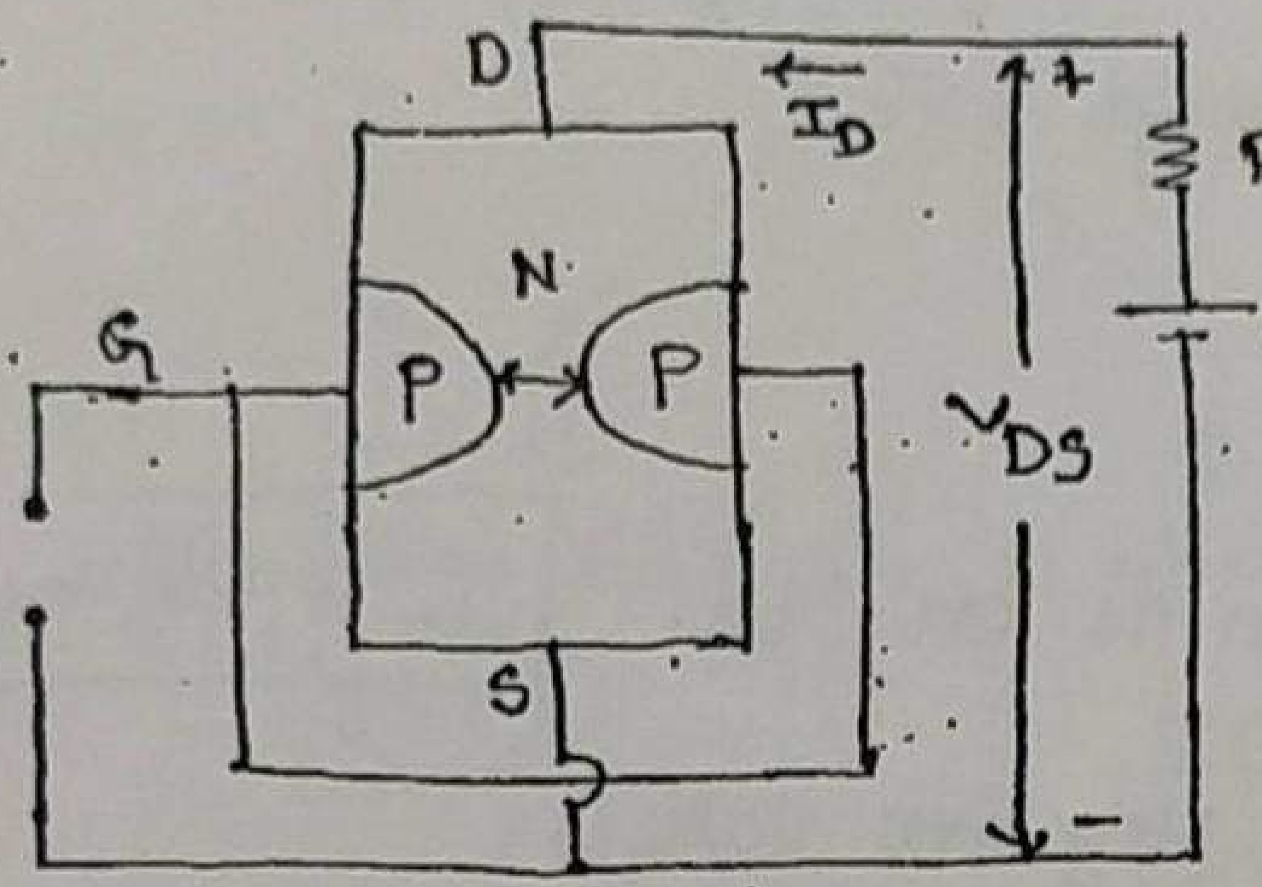
I_D vs V_{GS} when $V_{DS} = \text{const}$

- Transfer characteristics

Drain characteristics:-

I_D vs V_{DS} when V_{GS} = Const { (i). G & S → O.C ; (ii) G & S → S.C i.e V_{GS} = 0V ; (iii) $V_{GS} \neq 0V$ i.e V_{GS} -ve values.

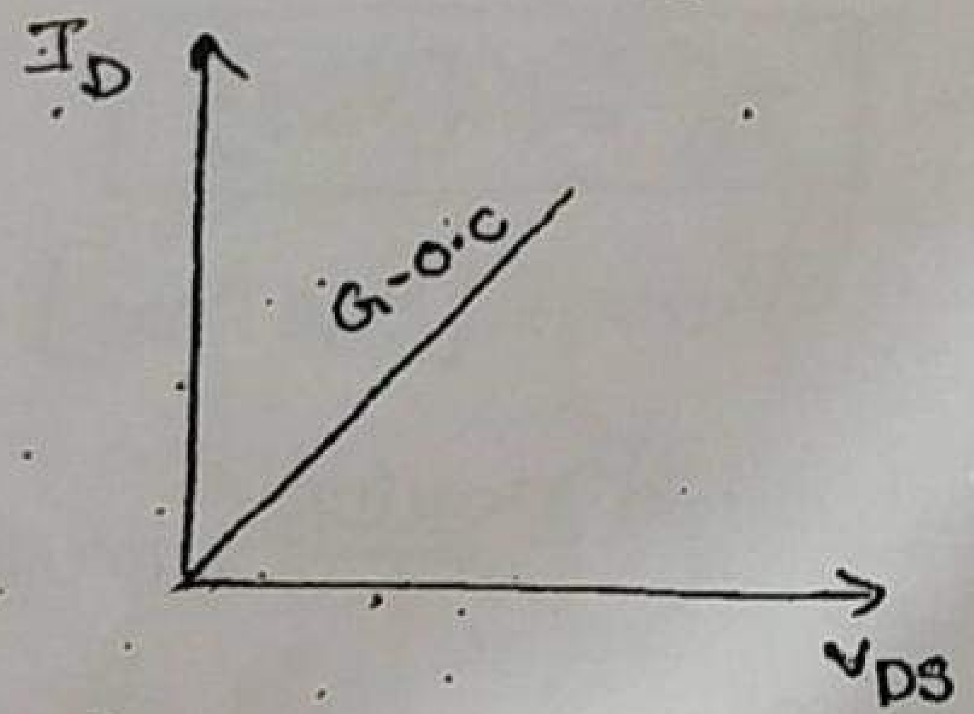
case (i):- when 'G' & 'S' → O.C



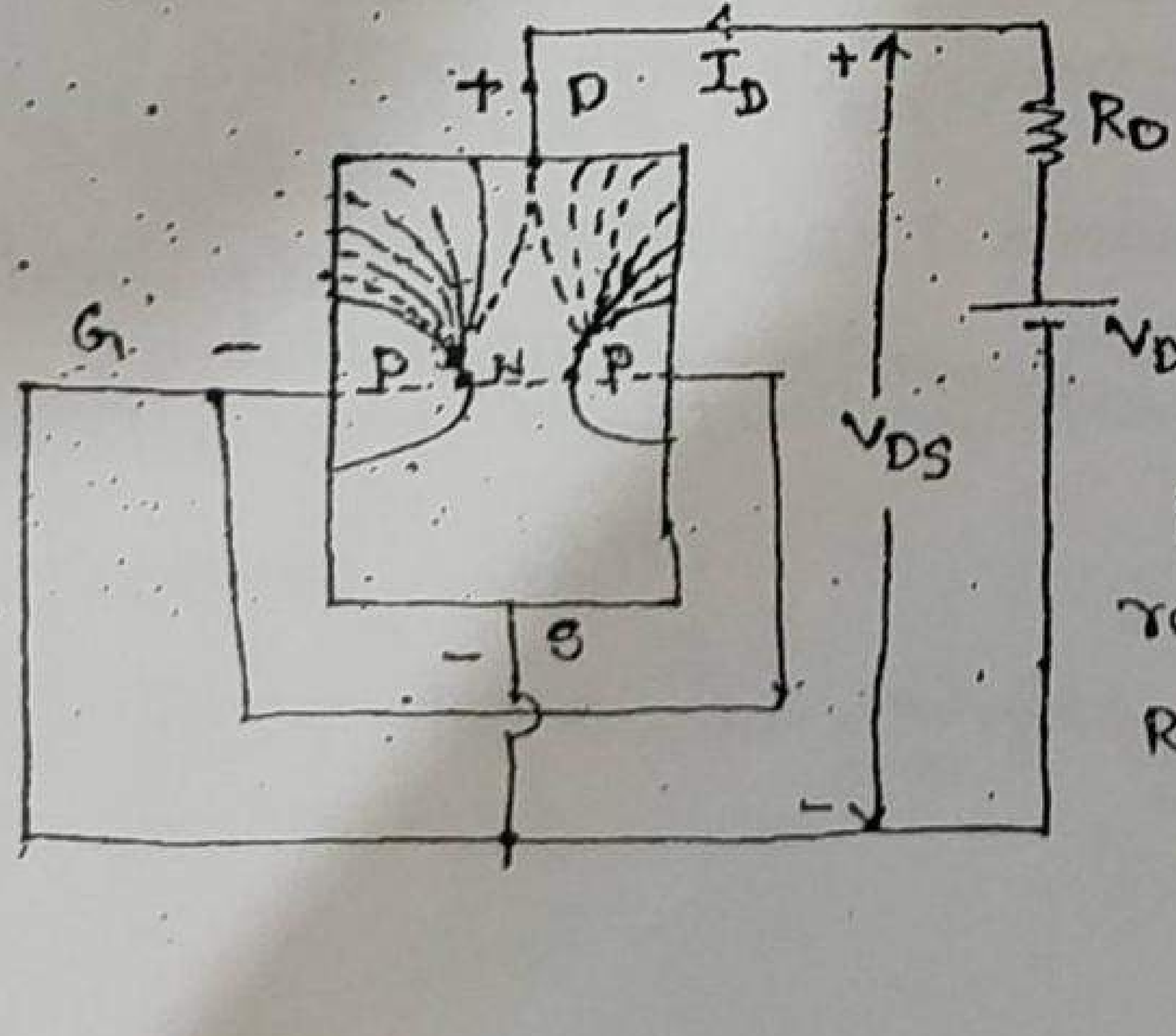
* AS Gate - O.C ;
The depletion region widths are fixed.
- Channel width constant.
- channel Resistance constant.

* when V_{DS}↑ I_D↑
The drain current increases in acc'n with the applied voltage V_{DS}.

* JFET acts as a <u>LINEAR RESISTOR</u> when Gate O.C



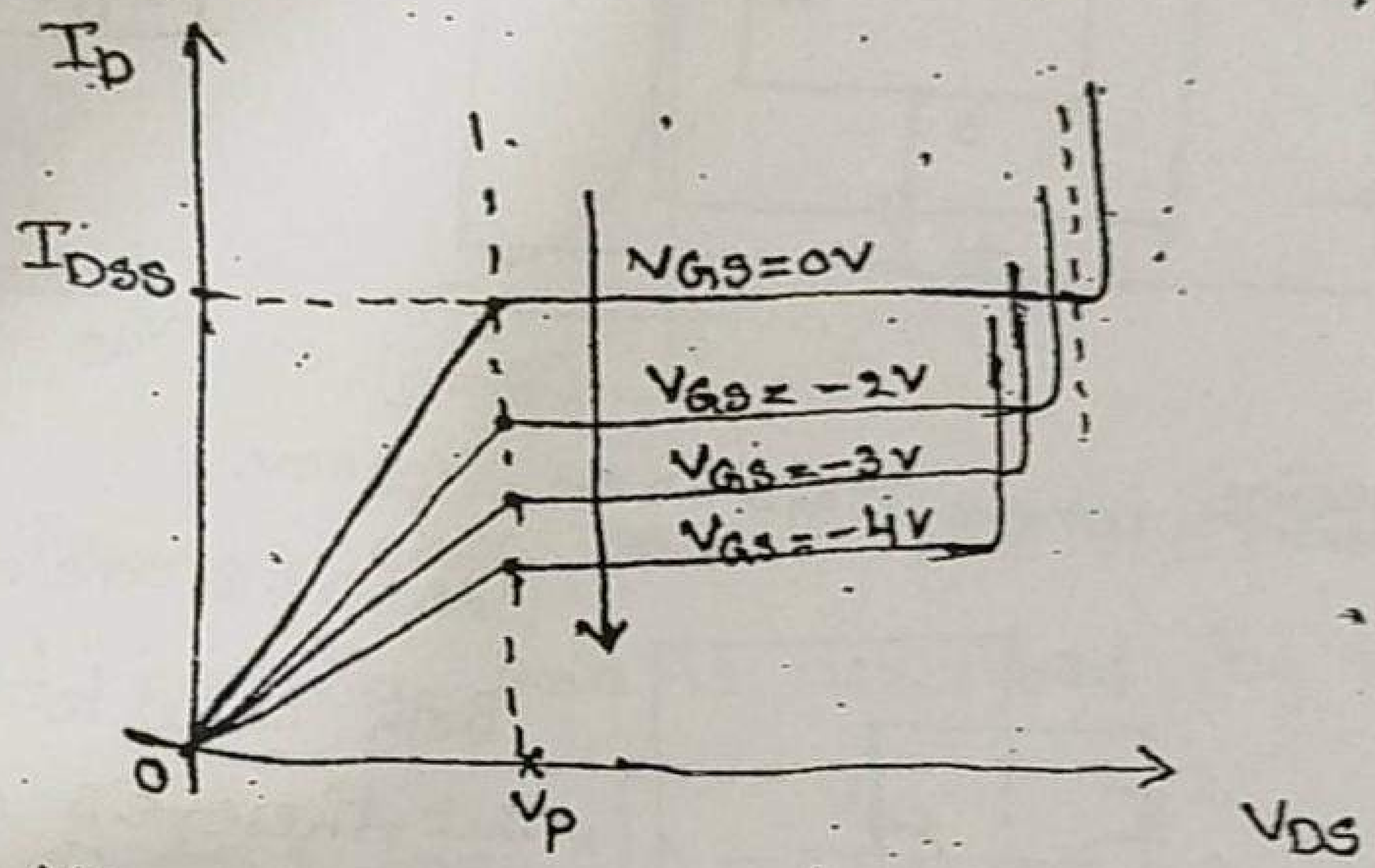
case (ii) when 'G' & 'S' terminals are S.C i.e V_{GS} = 0V.



* AS Gate & source — S.C ;
The lower half depletion region uneffected. The upper half depletion region effected :

* AS V_{DS}↑ I_D↑
AS V_{DS}↑ — the upper half dep. region widths↑. the channel Resistance ↑.
(R)

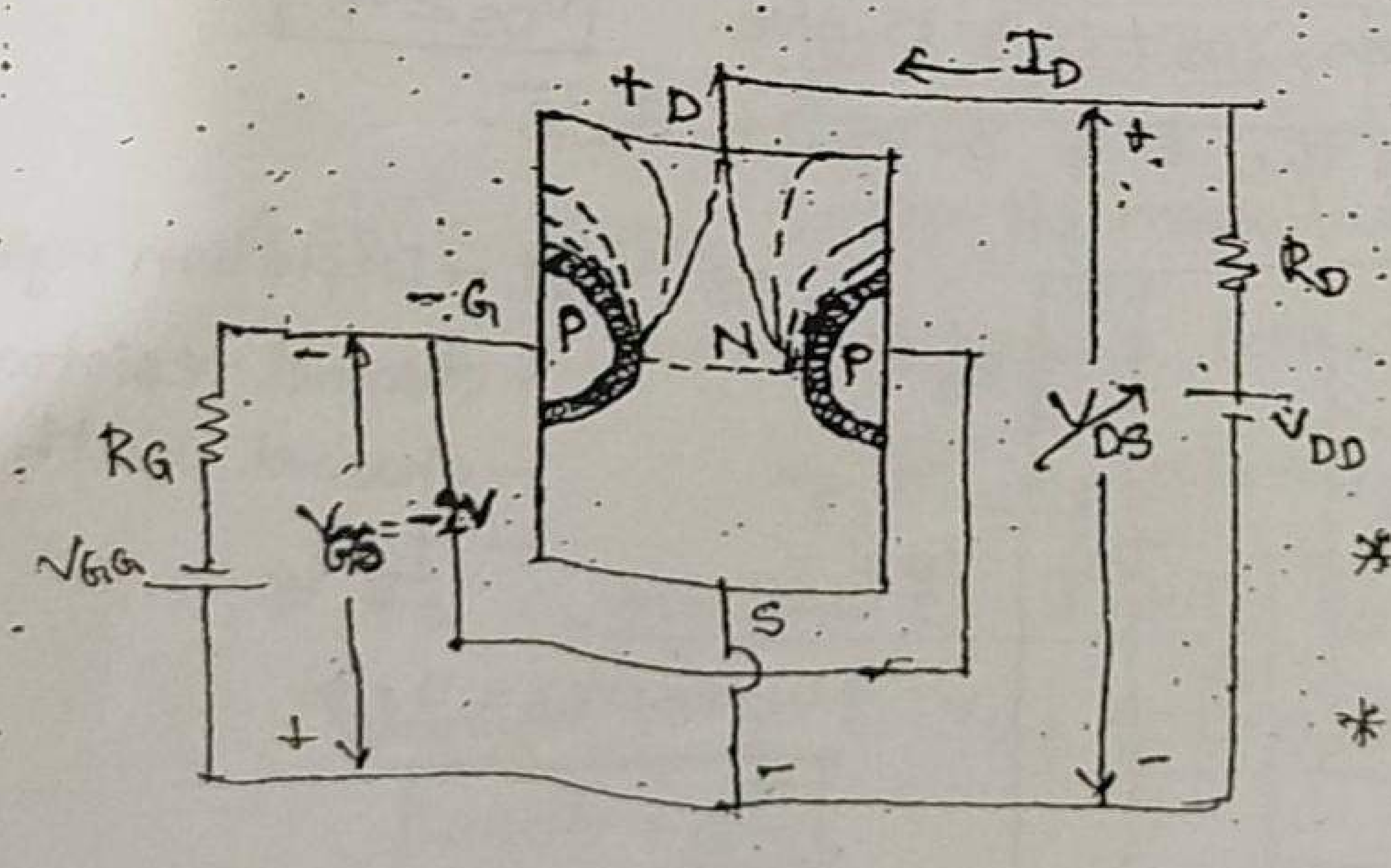
* $V_{DS}\uparrow$ $I_D\uparrow$ $R\uparrow$ upto pinch-off voltage (V_P) upto V_P, $I_D\uparrow$ in accordance with V_{DS}.
* Beyond V_P, channel Resistance varies in accordance with the voltage V_{DS}.
* Beyond V_P; $V_{DS}\uparrow \rightarrow I_D$ almost constant. $R\uparrow$
* Beyond V_P, $\rightarrow$ JFET acts as Voltage variable Resistor (or) VVR (or) V^2R.



when $V_{GS}=0V$ $\rightarrow$ The drain current is I_{DSS}.

I_{DSS} $\rightarrow$ Drain current when Source shorted to Gate.

Case(iii) :- when $V_{GS}\neq 0$; Let $V_{GS}=-2V$



For $V_{GS}=-2V$

$\rightarrow$ The depletion region widths $\uparrow$

$\rightarrow$ Channel width $\downarrow$

$\rightarrow$ $I_D\downarrow$

* The current is less than case (ii)
* As $V_{DS}\uparrow$ upto V_P $I_D\uparrow$ $R\uparrow$ (very small)

beyond V_P $I_D\rightarrow$ almost constant $R\uparrow$

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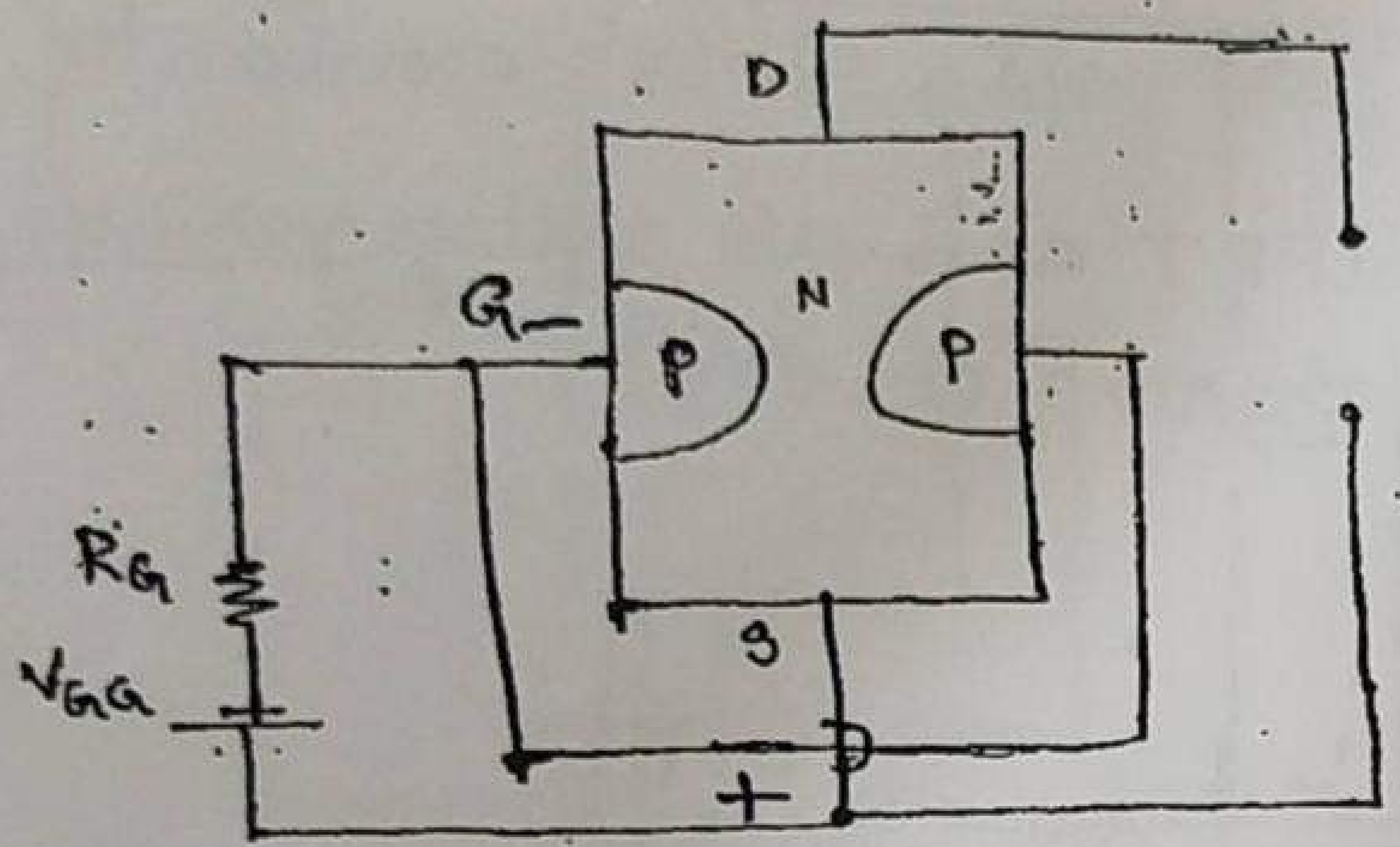
* As V_{GS} potential ↑ I_D ↓ ; As V_{DS} potential ↑ I_D ↑.

Transfer characteristics :-

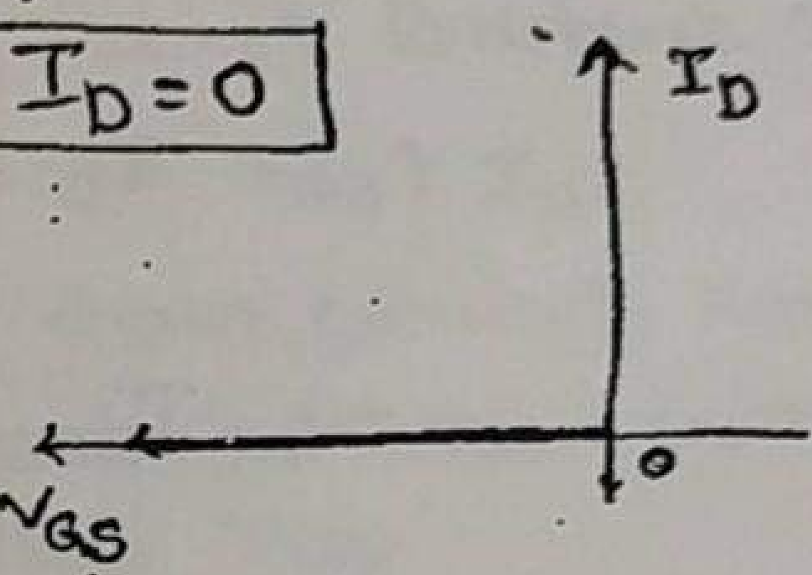
I_D vs V_{GS} when V_{DS} = const.
- (i) D & S → O.C
- (ii) D & S → S.C i.e V_{DS} = 0V
- (iii) $V_{DS} \neq 0V$

case (i) :- when 'D' & 'S' → O.C

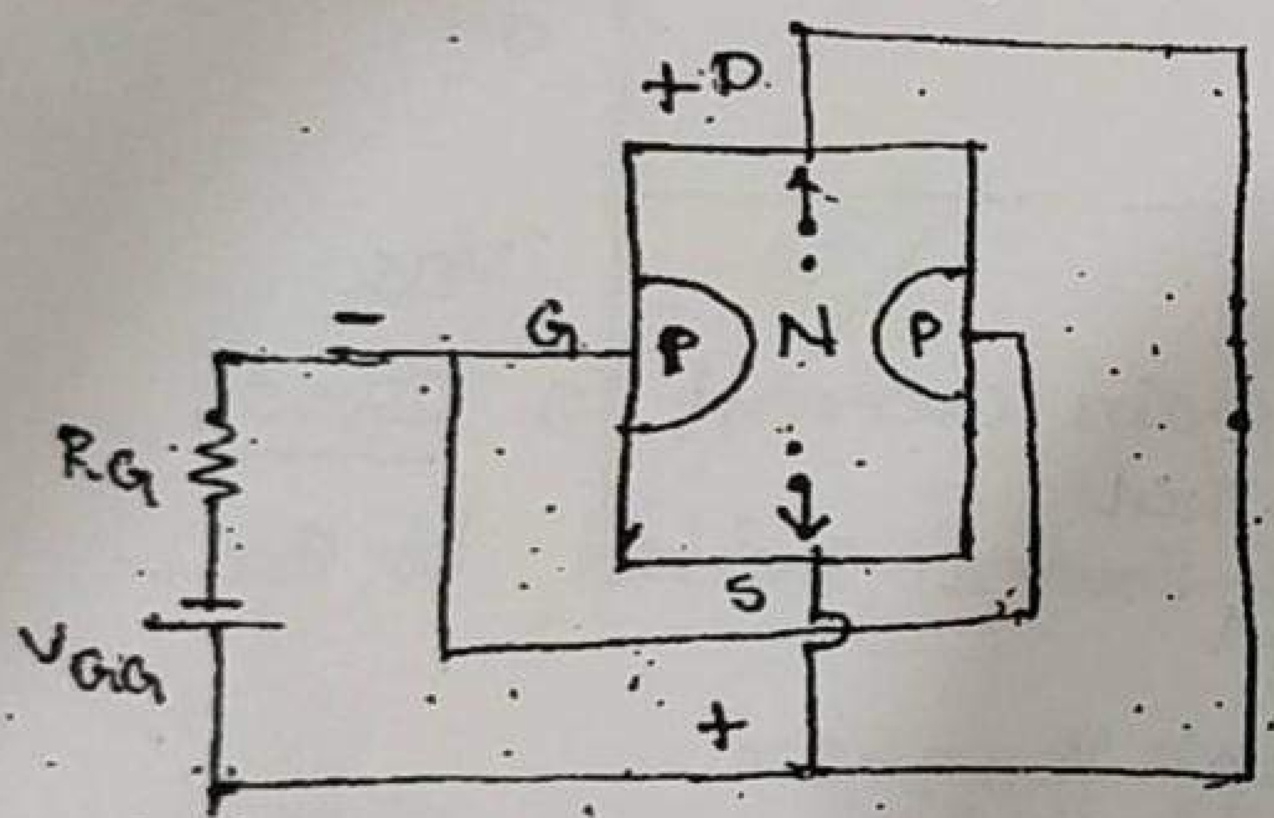


* As Drain → O.C
Drain terminal unable to collect the $\bar{e}$

$\boxed{I_D = 0}$



case (ii) :- when 'D' & 'S' → S.C V_{DS} = 0V.



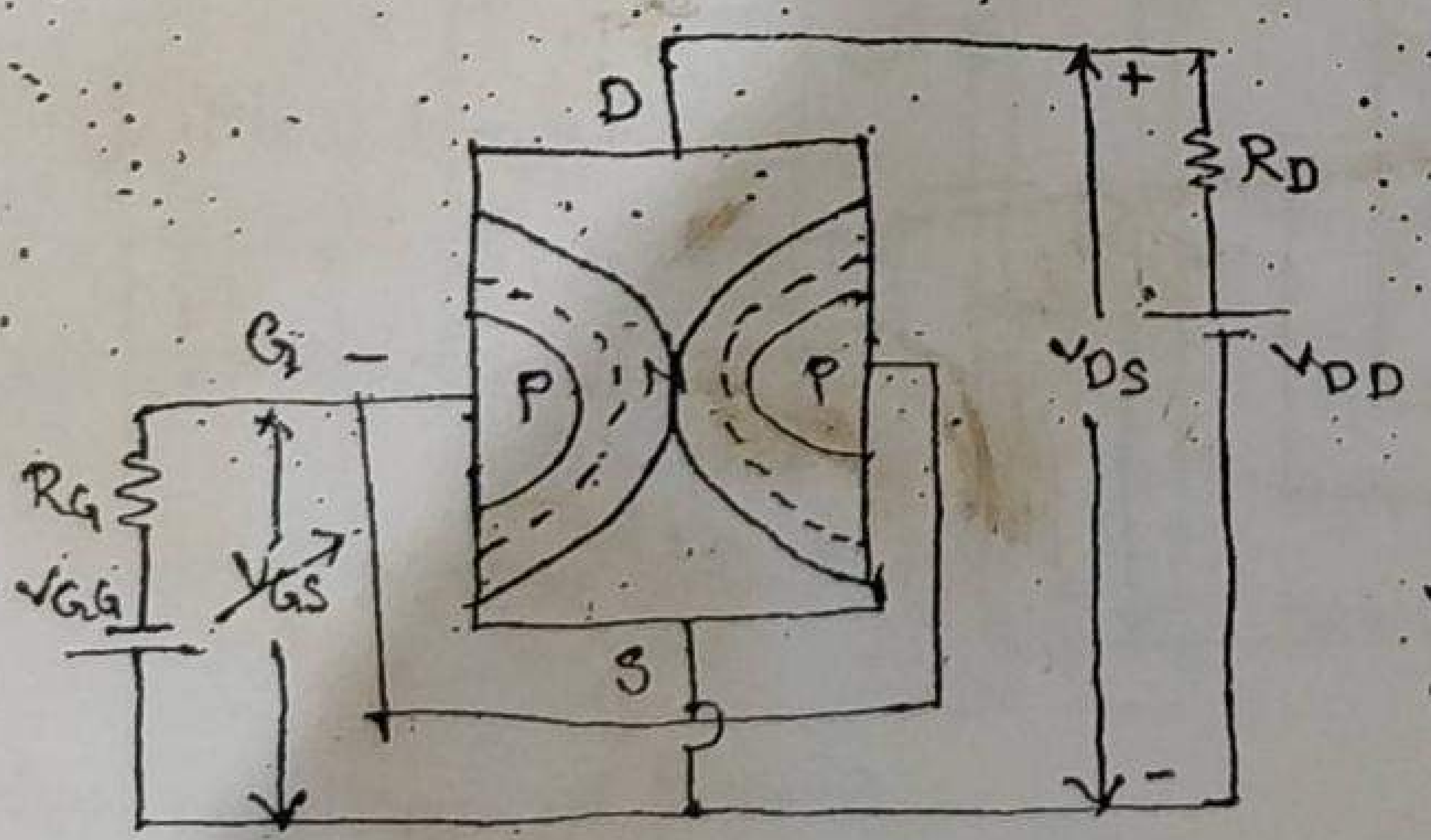
As D & S are at +ve.
Both able to attract the $\bar{e}$
But these $\bar{e}$s can't form loop

$\boxed{I_D = 0}$

As V_{GS} ↑ → $\boxed{I_D = 0}$.

case (iii) :- when $V_{DS} \neq 0$ & is +ve. $\boxed{V_{DS} \geq V_P}$

'D' - collects the $\bar{e}$ & S - emits the $\bar{e}$.



As V_{GS} ↑ → Depletion regions ↑
- channel resistance ↑
- channel width ↓
- I_D ↓

when $V_{GS} = 0$ ⇒

$\boxed{I_D = I_{DSS}}$

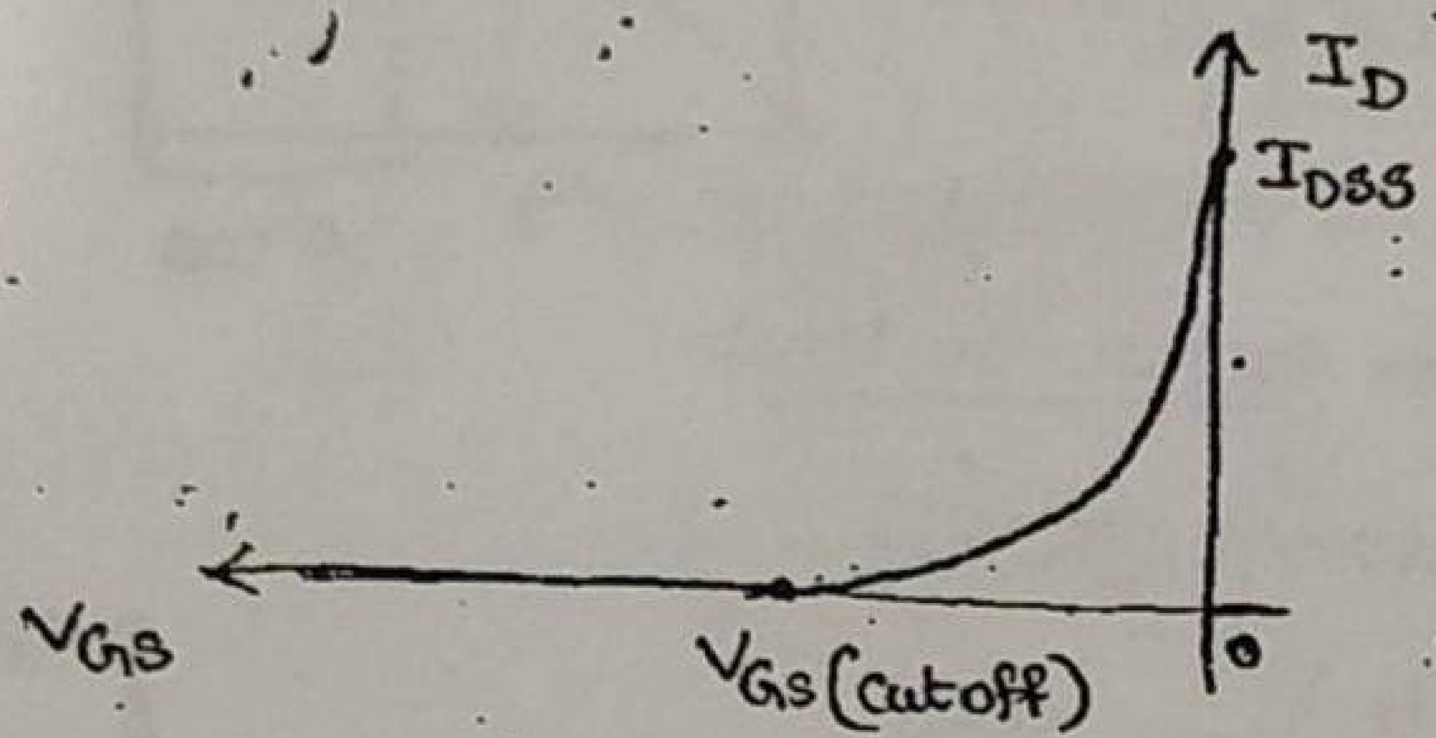
As $V_{GS}\uparrow$ $I_D\downarrow$

$V_{GS}\uparrow\uparrow$ $I_D\downarrow\downarrow$

At some particular voltage depletion region occupies the channel width $\Rightarrow$ channel width becomes zero

$\Rightarrow \boxed{I_D = 0}$ $\Rightarrow$ The JFET becomes "cutoff".

The potential is called V_{GS}(cutoff) voltage.



* The Transfer char. of the JFET in the shape inverted parabola. and is described by the equation

$$\therefore I_D = I_{DSS} \times \left[1 - \frac{V_{GS}}{V_{GS(cutoff)}}\right]^2$$

* when $V_{GS} = 0 \Rightarrow I_D = I_{DSS}$.

$V_{GS} = V_{GS(cutoff)} \Rightarrow I_D = 0$.

$$\boxed{0 < I_D < I_{DSS}}$$

* for a given JFET the magnitudes of pinch-off voltage and cut-off voltages are same.

$$V_P = |V_{GS}(\text{cut-off})|$$

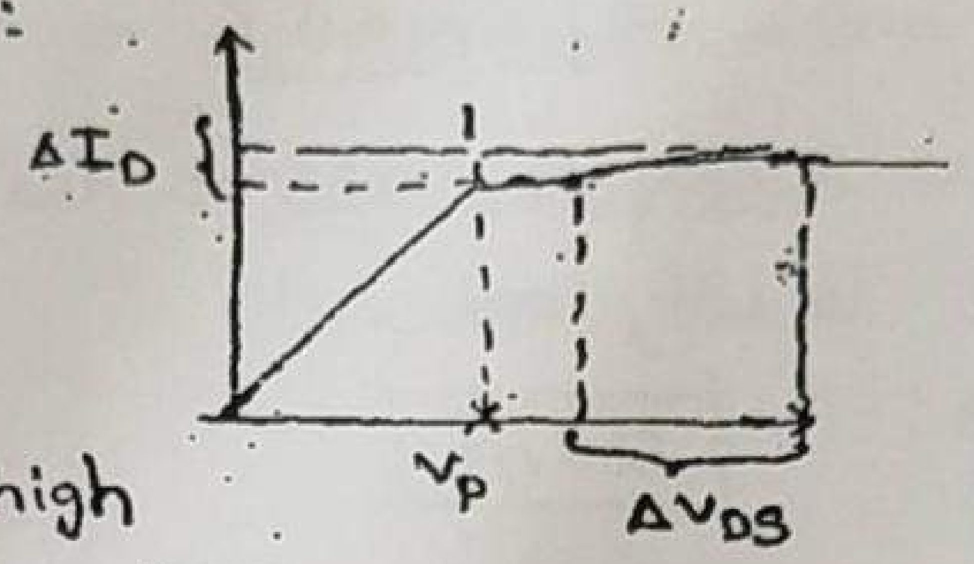
* for a N-channel JFET the pinch-off voltage (V_P) is always +ve & V_{GS} (cutoff) is always -ve.

JFET Parameters:-

The JFET Parameters are
(i) Drain Resistance (r_d).
(ii) Transconductance (g_m).
(iii) Amplification factor (μ).

1. Drain Resistance (r_d):

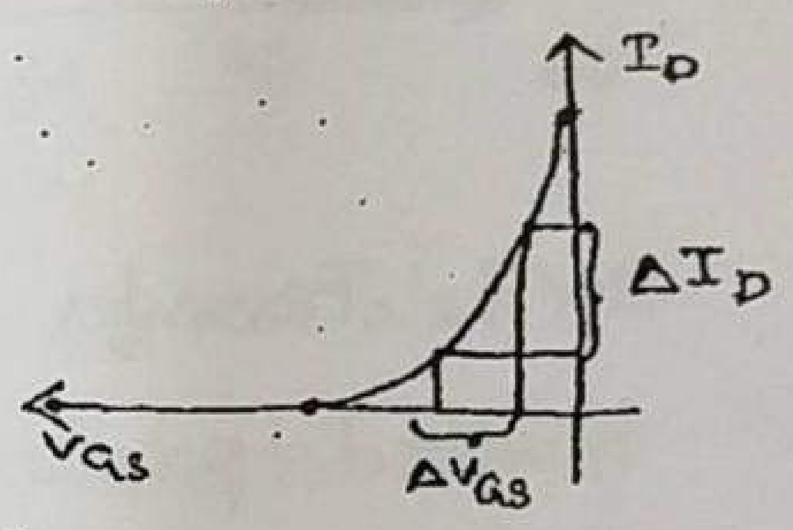
$$\boxed{r_d = \left[\frac{\Delta V_{DS}}{\Delta I_D}\right]}$$



for a JFET $r_d \rightarrow$ very high
r_d ranges from 100kΩ to 1MΩ.

2. Transconductance (g_m):-

$$g_m = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) \text{ (or) } \frac{dI_D}{dV_{GS}}$$



The drain current of the JFET is

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(cutoff)}}\right]^2$$

diff w.r.t V_{GS}

$$\frac{dI_D}{dV_{GS}} = I_{DSS} \times 2\left[1 - \frac{V_{GS}}{V_{GS(cutoff)}}\right]\left[-\frac{1}{V_{GS(cutoff)}}\right]$$

$$\boxed{g_m = -\frac{2I_{DSS}}{V_{GS(cutoff)}}\left[1 - \frac{V_{GS}}{V_{GS(cutoff)}}\right]}$$

3. Amplification factor:-

$$\boxed{\mu = \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)}$$

$$\mu = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) \times \left(\frac{\Delta V_{DS}}{\Delta I_D}\right)$$

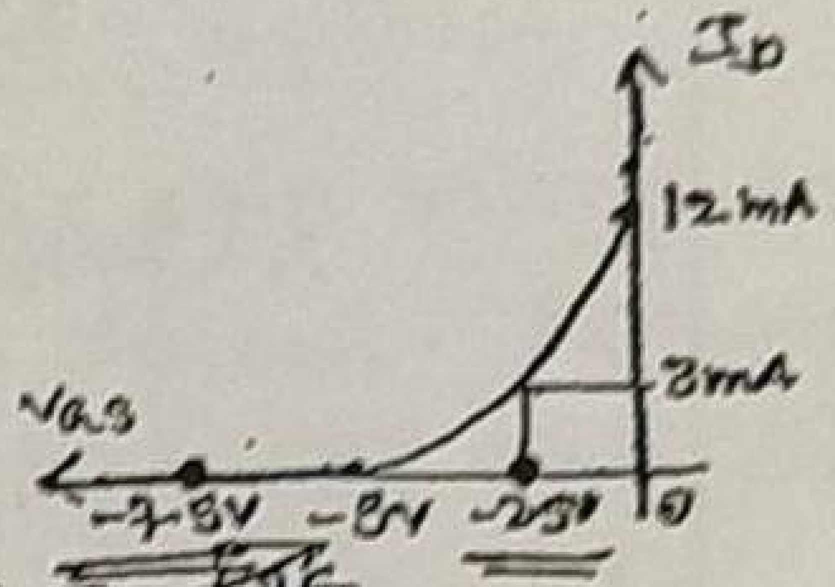
$$\boxed{\mu = g_m \times r_d}$$

Pb:- An n-channel JFET has $I_{DSS} = 12mA$ the $V_P = 5V$ calculate the require value of V_{GS} voltage to get $I_D = 3mA$.

Sol:-

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(cutoff)}}\right]^2$$

$$\cancel{3}mA = \overset{4}{\cancel{12}}mA\left[1 - \frac{V_{GS}}{-5V}\right]^2$$



$$\cancel{(5 - V_{GS})^2 = \frac{3mA \times 25V}{12mA}}$$

$$\cancel{5 - V_{GS} = \sqrt{\frac{25}{4}}}$$

$$\frac{1}{4} = \left(1 + \frac{V_{GS}}{5}\right)^2$$

$$1 + \frac{V_{GS}}{5} = \pm \frac{1}{2} \quad \Rightarrow \frac{V_{GS}}{5} = -0.5V, -1.5V$$

$$\frac{V_{GS}}{5} = \pm \frac{1}{2} - 1$$

$$\boxed{V_{GS} = -2.5V, \cancel{-7.5V}}$$

$$\boxed{V_{GS} = -2.5V}$$

Pb:- An n-channel JFET has the $V_P = -6V$ the JFET offers a trans conductance (g_m) of 3m℧ when $V_{GS} = -1.5$ calculate

1. The max transconductance offered by the JFET.
2. Drain current when $V_{GS} = -2V$.

Sol:-

$$g_m = \frac{-2 I_{DSS}}{V_{GS(cutoff)}}\left[1 - \frac{V_{GS}}{V_{GS(cutoff)}}\right]$$

$$(g_m)_{max}\Big|_{V_{GS}=0} \qquad \boxed{(g_m)_{max} = \frac{-2 I_{DSS}}{V_{GS(cutoff)}}}$$

$$g_m = \frac{-2 I_{DSS}}{V_{GS(cutoff)}}\left[1 - \frac{V_{GS}}{V_{GS(cutoff)}}\right]$$

$$3\times10^{-3} = \frac{+\cancel{2}\, I_{DSS}}{+\cancel{6}\,3}\left[1 - \frac{+1.5}{+\cancel{6}\,4}\right]$$

$$3m = \frac{I_{DSS}}{3}\left[\frac{3}{4}\right] \Rightarrow \boxed{I_{DSS} = 12mA}$$

$$\therefore (g_m)_{max} = \frac{+\cancel{2}\times \cancel{12}^{4}\times10^{-3}}{+\cancel{6}\,\cancel{3}} = 4m\mho.$$

(ii) $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(cutoff)}}\right]^2$$

$$= 12\times10^{-3}\left[1 - \frac{-2}{-6}\right]^2$$

$$= 12\times10^{-3}\left[\frac{2}{3}\right]^2$$

$$= 12\times\frac{4}{9}\,mA$$

$$= 5.33\,mA.$$

MOSFET:-

→ Metal oxide semi conductor FET.

Depletion MOSFET:

→ There channel exists b/w 'S' & 'D' terminals.

There is no necessity to apply a particular voltages b/w 'G' & 'S'.

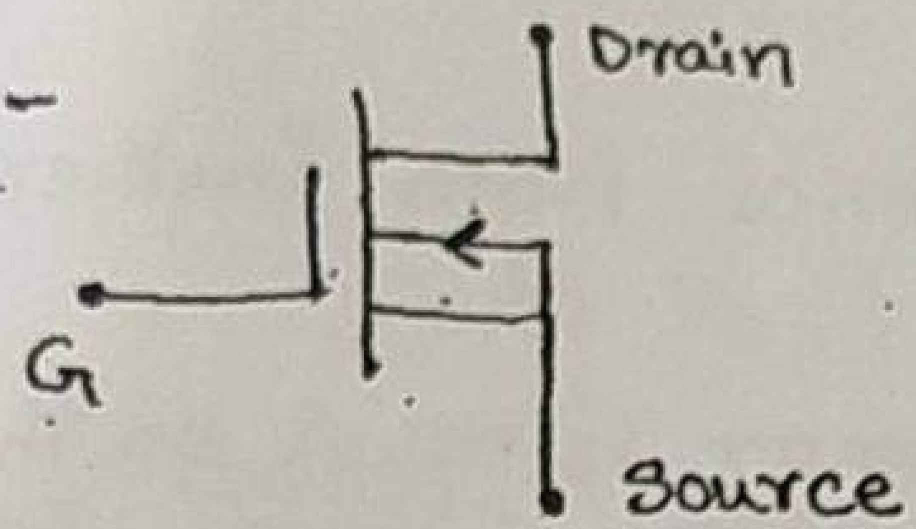
Enhancement MOSFET:

1. In E-MOSFET, no channel exists b/w 'S' & D terminals. There is a necessity to induce the channel b/w 'S' & D. To induce the channel b/w 'S' & D we must apply a proper potential b/w G & S terminals.

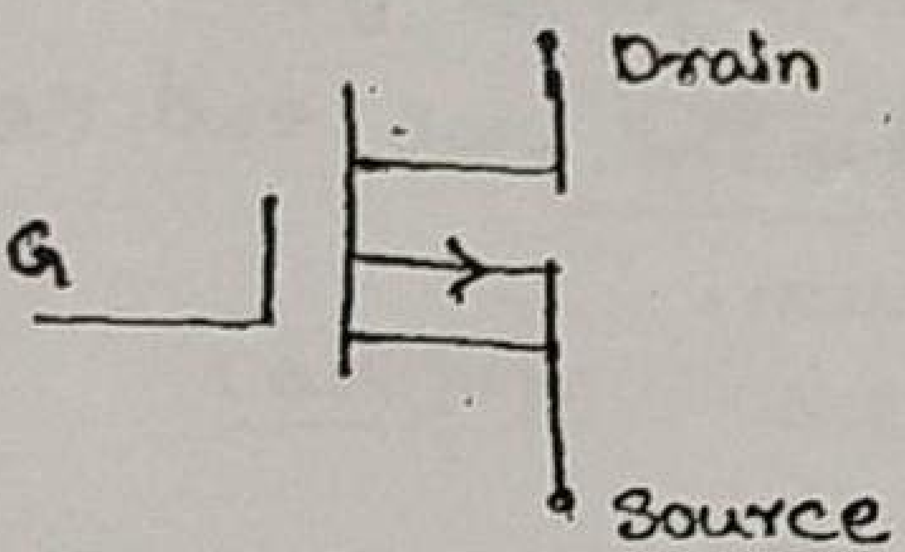
<u>Depletion MOSFET</u>

- we can apply any potentials b/w 'G' & 'S'.

$$V_{GS} \left\{ \begin{array}{l} +ve \text{ voltages} \\ 0 \text{ volts} \\ -ve \text{ voltages} \end{array} \right\}$$



N - channel D-MOSFET.



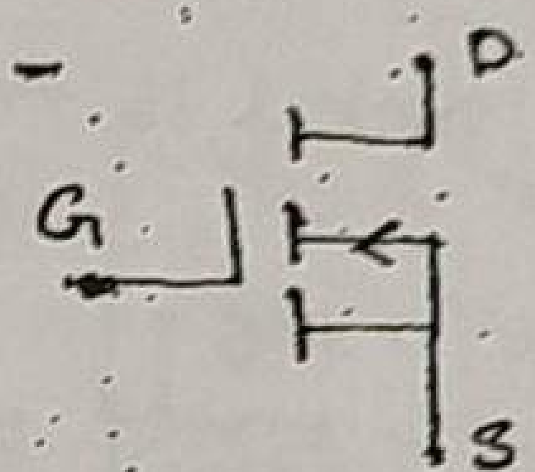
P-channel D- MOSFET

<u>Enhancement MOSFET.</u>

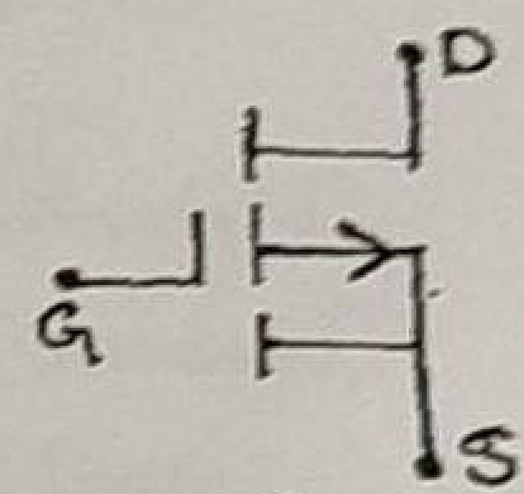
- for N-channel E-MOSFET
 * V_{GS} is always +ve. & $\underline{V_{GS} \geq V_{GS}}$ (threshold)

- when $\underline{V_{GS} = V_{GS}(th)}$:-

This is the min voltage to induce the channel. The channel is formed by a min no. of charg particles once channel formed by the charged particles, these charged particles are remains fixed for entire operation.



(N-ch-E-MOSFET)



(P-channel E-MOSFET)

Construction of N-channel MOSFET:-

MOSFET - (metal oxide semi conductor FET)

→ In the construction of N-Channel MOSFET, we are selecting the p-type substrate. The substrate is used to protect the device from the applied electric fields.

→ Two heavily dopped N-type sections are diffused into the substrate by maintaing the proper gap.

→ The gap b/w two N-sections is called "channel length" (or) space.

∴ Channel length = 1 mil → length - $= 1 \times 10^{-3} \times 2.54 \times 10^{-2} m$
$= 2.54 \times 10^{-5} m$
$= 25.4\, \mu m \simeq \underline{\underline{26\, \mu m}}$

→ The depletion regions formed under open ckt condition only..

→ one acts as source and another is acts as Drain.

→ over the surface of substrate an oxide layer is grown except where source & drain maintain to be contact.

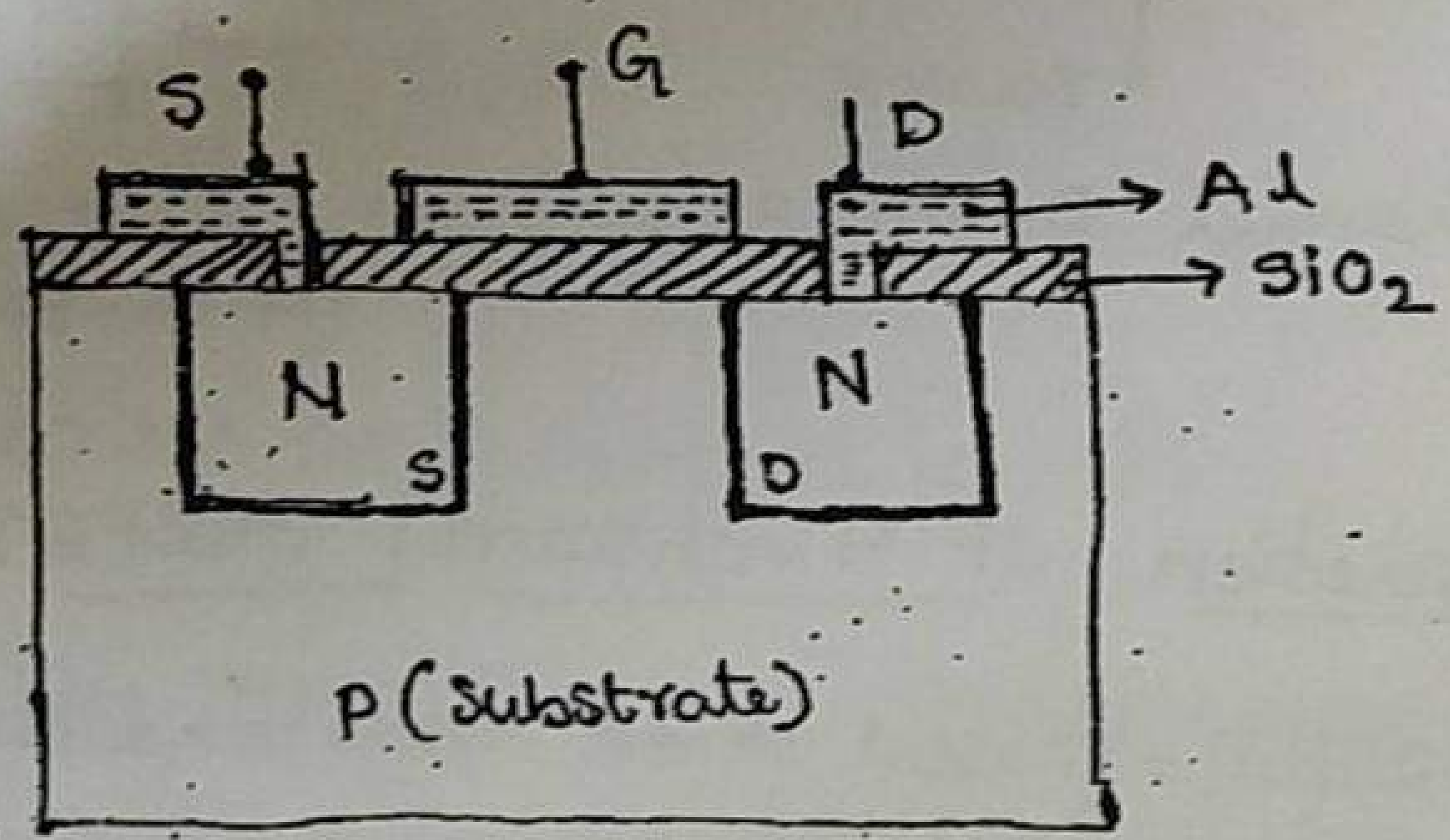
→ SiO_2: Dielectric material It's resistance is veryhigh (10^{10} to $10^{5}\Omega$).

→ This layer protects the device from further fabrication steps.

→ The i/p resistance of MOSFET is equal to the resistance of SiO_2

→ over this surface a metal layer is grown that must cover the entire space b/w the two end sections.

This metal is — Aluminum.



E-MOSFET characteristics:-

$$I_D = f\,[V_{GS}; V_{DS}]$$

* I_D vs. V_{DS} when V_{GS} = const

→ Drain characteristics.

* I_D vs. V_{GS} when V_{DS} = Const

→ Transfer characteristics.

1. Drain Characteristics:

I_D vs V_{DS} when V_{GS} = constant
- (i) 'G' & 'S' → O.C
- (ii) 'G' & 'S' → S.C i.e $V_{GS}=0V$
- (iii) $V_{GS} \neq 0$.

Case(i) when 'G' & S → O.C

As Gate O.C → No channel formed b/w 'D' & 'S' terminals.

$\boxed{I_D=0}$

As $V_{DS}\uparrow \Rightarrow \boxed{I_D=0}$

Case(ii):- when G & S → S.C. i.e $V_{GS}=0V$.

As $V_{GS}=0V$, No channel formed b/w 'S' & 'D'

$\boxed{I_D=0}$, As $V_{DS}\uparrow \Rightarrow \boxed{I_D=0}$

Case(iii):- when $V_{GS}\neq 0$.
- $V_{GS} < V_{GS}$ (threshold)
- $V_{GS} = V_{GS}$ (threshold)
- $V_{GS} > V_{GS}$ (threshold)

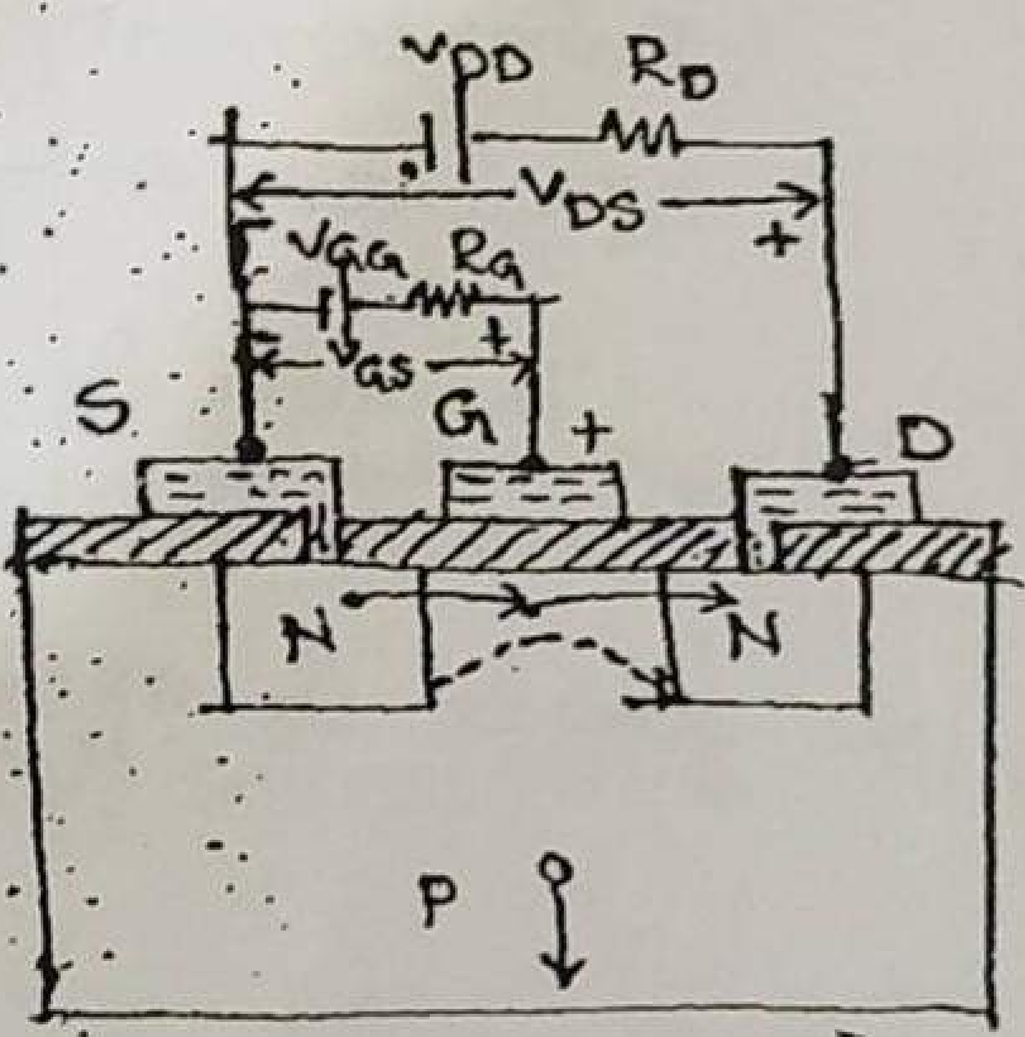
(a) for $V_{GS} < V_{GS(th)}$

- No channel is formed $\boxed{I_D=0}$

As $V_{DS}\uparrow$ $\boxed{I_D=0}$

(b) As $V_{GS} = V_{GS(th)}$

At this potential channel is formed.

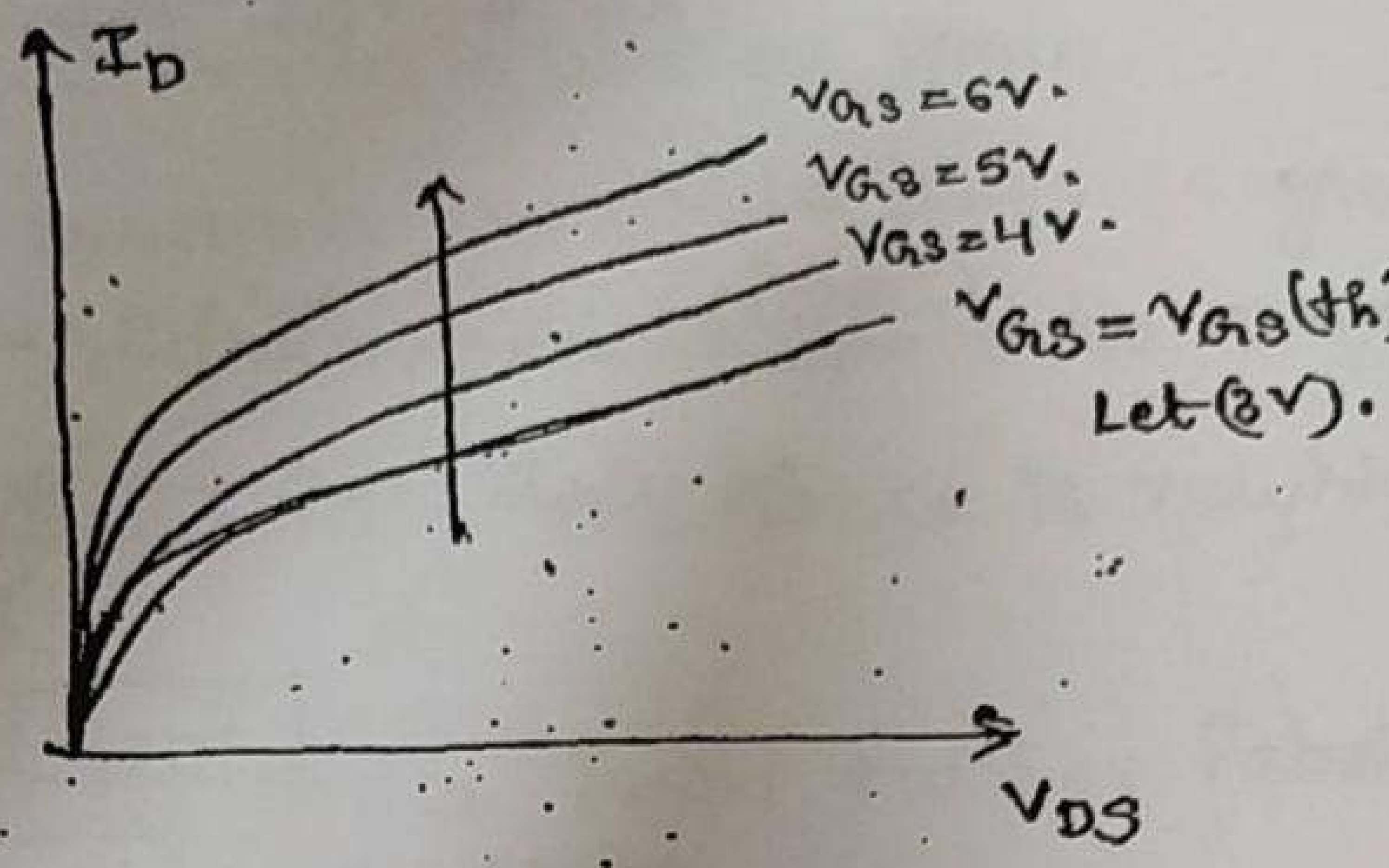


* Due to parallel plate effect, the minority carriers ($\bar{e}$s) of substrate comes b/w 'S' & 'D' and forms a layer called INVERSION LAYER.
* These $\bar{e}$s are remains fixed for entire operation.

As $V_{DS}\uparrow$

source emits the $\bar{e}$s & 'D' collects these $\bar{e}$.

As $V_{DS}\uparrow$ $I_D\uparrow$



(c) As $V_{GS} > V_{GS}(th)$ Let $V_{GS}=4V$

Due to parallel plate effect some more $\bar{e}$ enters into the channel, & are considered as free $\bar{e}$s.

when V_{DS} applied — Drain able to collect these $\bar{e}$s & the $\bar{e}$s from source.

Now I_D is more in this case compared to case(b)

As $V_{DS}\uparrow$ $I_D\uparrow$.

The mode of operation in which the drain current increases as the V_{GS} voltage increases is called Enhancement mode of operation. The E-MOSFET operated ~~only~~ in Enhancement mode only.

The mode of operation in which the Drain current decreases as V_{GS} voltage increases is called Depletion mode of operation. Ex:- JFET.

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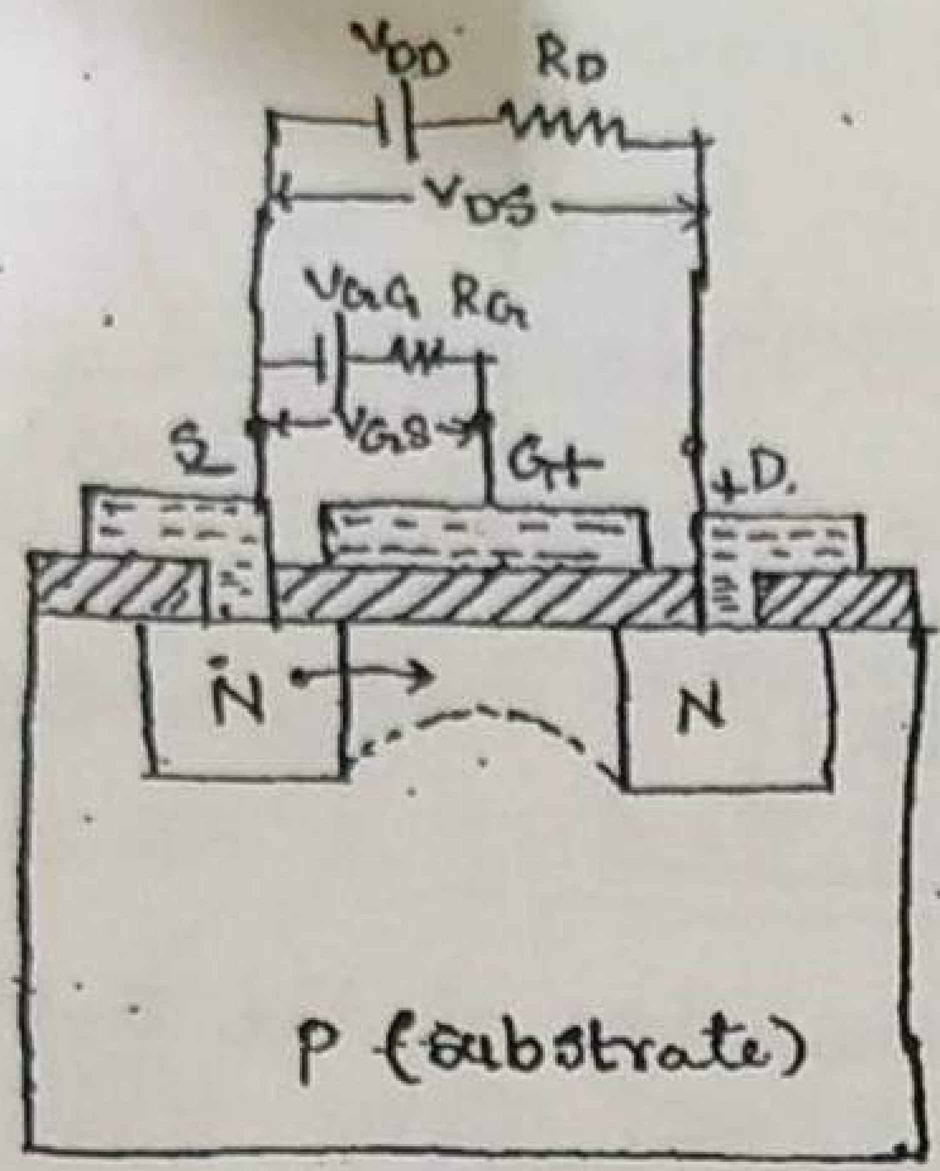
2. Transfer characteristics:-

I_D vs V_{GS} when V_{DS} = constant
(i) 'D' & S → O.C
(ii) 'D' & S → S.C i.e V_{DS} = 0V.
(iii) $V_{DS} \neq 0V$.



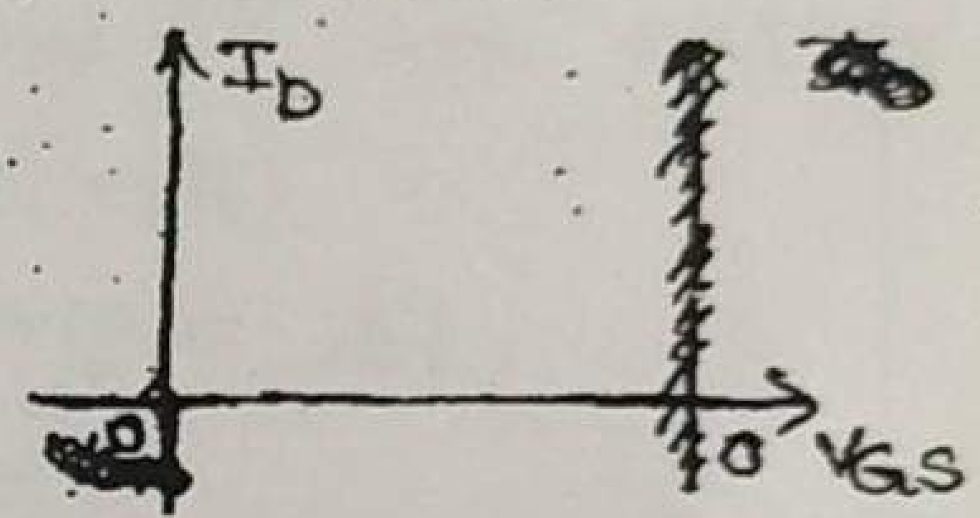
case (i). when D & S → O.C

As 'D' — O.C.

Drain unable to collect the charged particles.

$\boxed{I_D = 0}$

As V_{GS}↑ → $\boxed{I_D = 0}$



case (ii):-

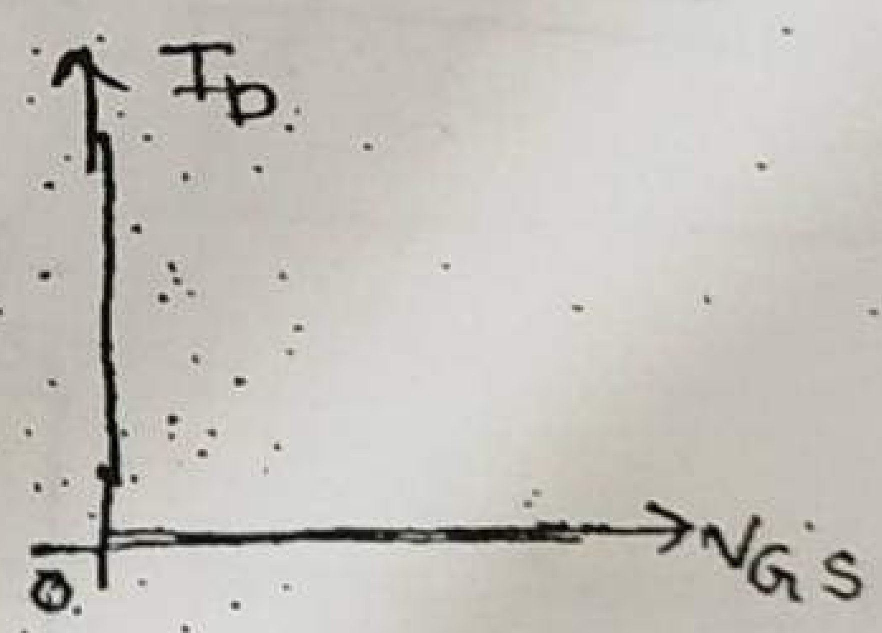
when D & S → S.C

$\boxed{V_{DS} = 0V}$

The drain terminal repels the ē's which are emitted from source. These ē's cannot form the closed loop.

$\boxed{I_D = 0}$

As V_{GS}↑ → $I_D = 0$



case (iii):- when $V_{DS} \neq 0$.

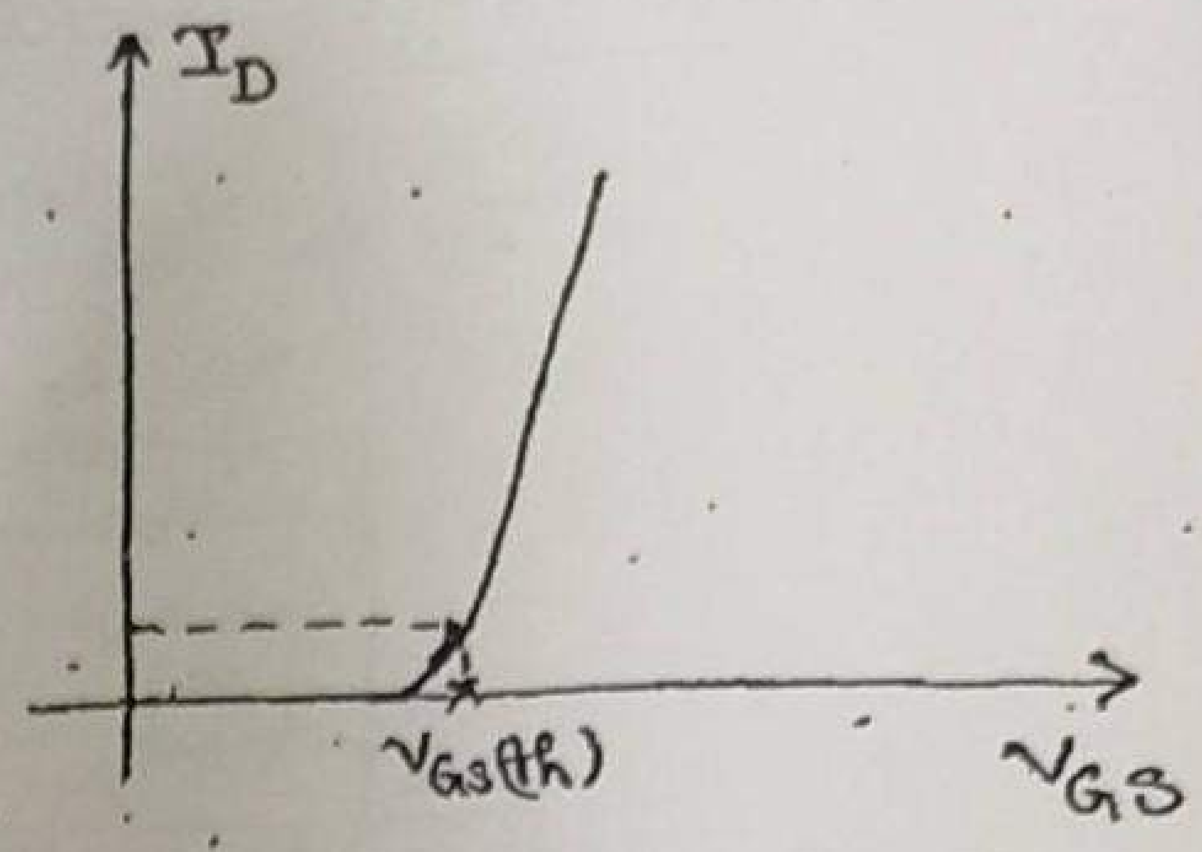
Drain at higher potential than 'S'. source emits the ē's and drain collects these ē's.

As V_{GS}↑
- $V_{GS} < V_{GS}(th)$ → No channel formed → $I_D = 0$.
- $V_{GS} = V_{GS}(th)$ → $I_D \neq 0$
- $V_{GS} > V_{GS}(th)$

As $V_{GS} \uparrow$ beyond the $V_{GS}(th)$

The drain current $\uparrow$

$\therefore V_{GS} \uparrow \; I_D \uparrow$.



The drain current I_D through the E-MOSFET follows the eqn.

$$\boxed{I_D = K\left[V_{GS} - V_{GS}(th)\right]^2} \qquad V_{GS} > V_{GS}(th)$$

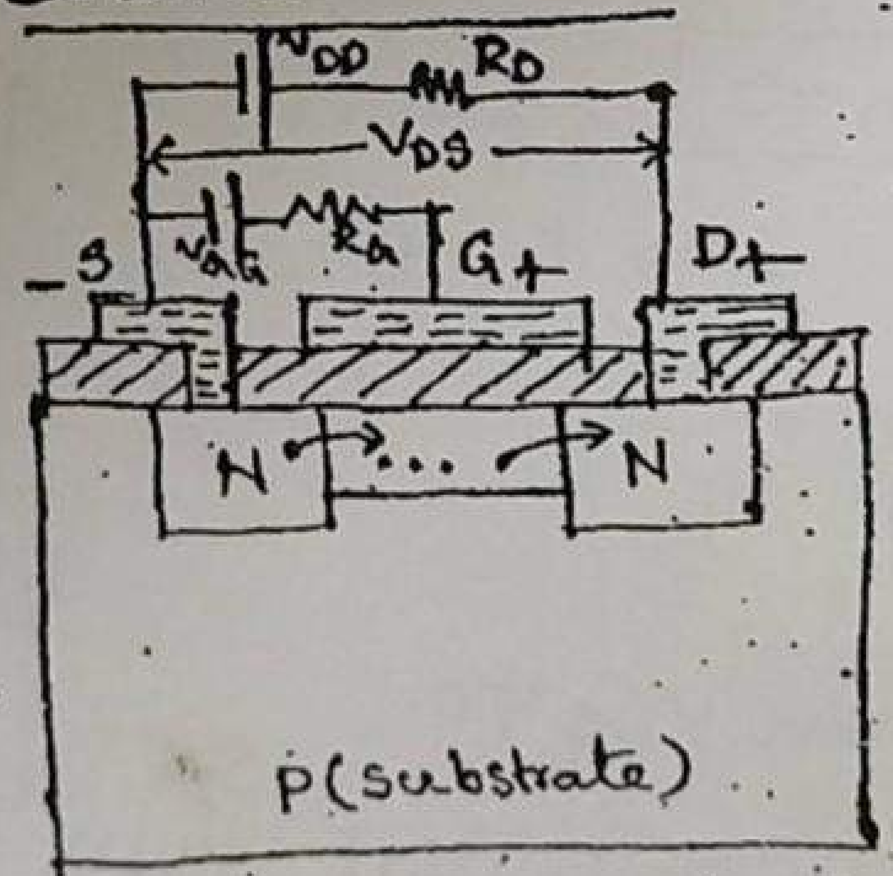
where $K \rightarrow$ parameter of the E-MOSFET &

whose value is $K = \dfrac{I_D(ON)}{\left[V_{GS}(ON) - V_{GS}(th)\right]^2}$

For a given E-MOSFET

$\left\{ \begin{matrix} I_D(ON),\ V_{GS}(ON)\ \& \\ V_{GS}(th) \end{matrix} \right\}$ values will be given.

D-MOSFET: Characteristics:-



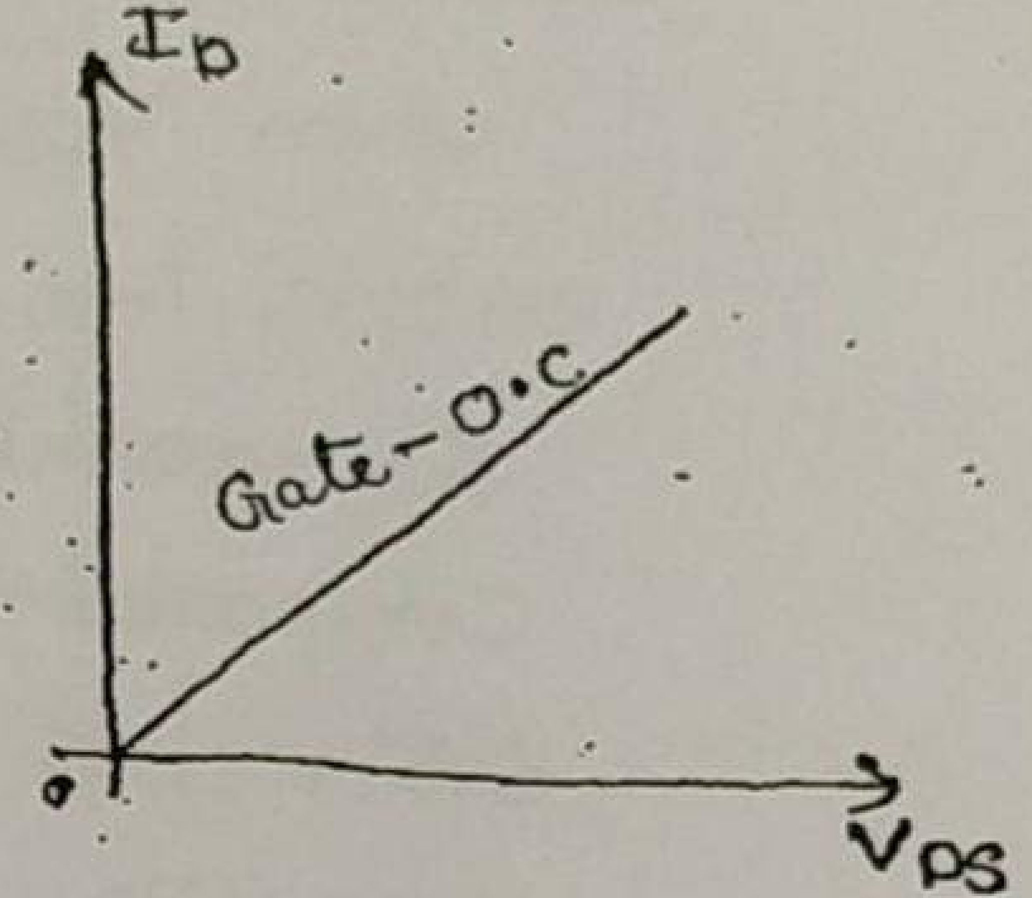
Drain characteristics:-

I_D vs V_{DS} when V_{GS} = const $\begin{cases} \text{(i) } G \,\&\, S \rightarrow O.C \\ \text{(ii) } G \,\&\, S \rightarrow S.C \rightarrow V_{GS} = 0V \\ \text{(iii) } V_{GS} \neq 0V \text{ i.e. } +ve \,/\, -ve \end{cases}$

case (i): when G & S $\longrightarrow$ O.C

AS G-O.C → Due to parallel plate no charged particles enters into channel.

* when V_{DS} applied, source emits the $\bar{e}$s and these $\bar{e}$s are collected by Drain
* when G → O.C. → D-MOSFET acts as a LINEAR Resistor.

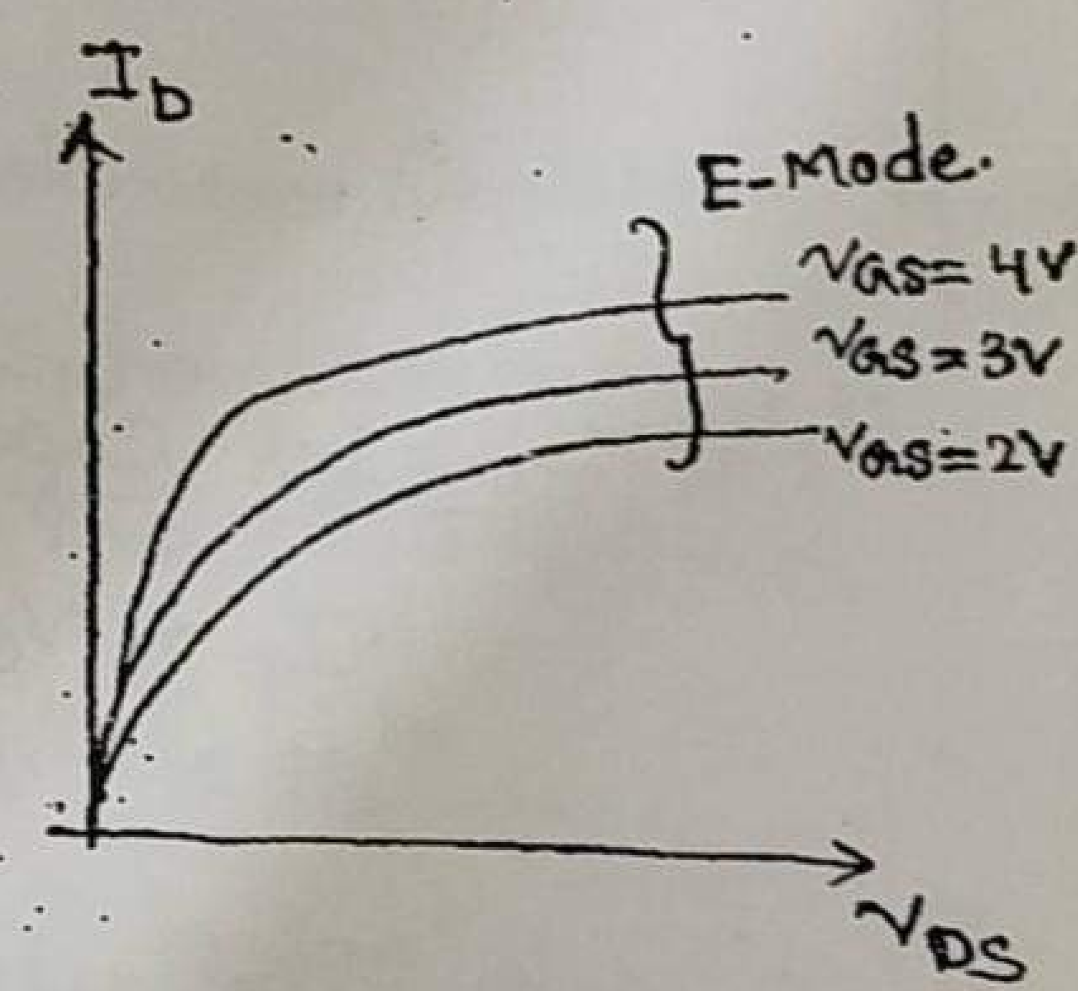


case (ii):- when V_{GS} +ve

Due to parallel plate effect some $\bar{e}$s are entered into the channel from the substrate.

when V_{DS} applied, drain able to collect the $\bar{e}$s from source and the $\bar{e}$s from channel which are entered from substrate.

As $V_{DS}\uparrow$ $I_D\uparrow$



case (iii):- when V_{GS} = 0V

* Due to parallel plate effect some holes enters into the channel from substrate.
* when V_{DS} applied, source emits the $\bar{e}$s & these $\bar{e}$ enters into channel & recombine with holes. The remaining $\bar{e}$s are collected by the drain.

∴ The drain collects the no. of $\bar{e}$s less than the no. of $\bar{e}$s emitted by source.

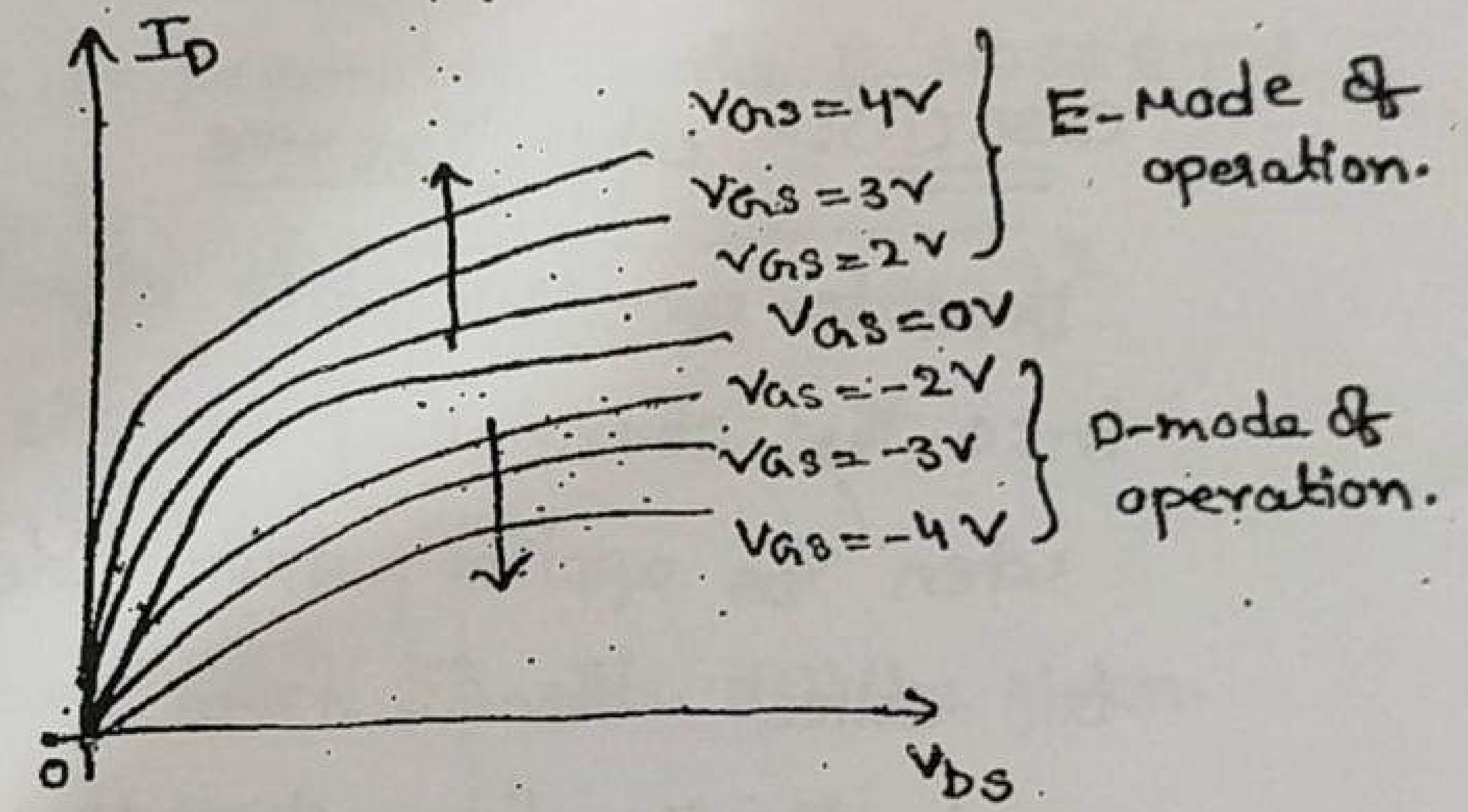
- I_D is less in this case compared to case (ii).

case (iv):- when V_{GS} -ve

Due to parallel plate effect the no. of holes enters into channel more in this case compared to case (iii).

when V_{DS} applied, the $\bar{e}$ emitted from source enters into channel and recombine with holes.

The recombination rate in this case is more compared to case (iii). The no. of $\bar{e}$s collected by drain less I_D is less in this case compared to case (iii).



Transfer characteristics:-

I_D vs V_{GS} when V_{DS} = const $\begin{cases} \text{(i) D \& S} \rightarrow \text{O.C} \\ \text{(ii) D \& S} \rightarrow \text{S.C i.e. } V_{DS}=0V \\ \text{(iii) } V_{DS} \neq 0V. \end{cases}$ $\rightarrow I_D = 0A$

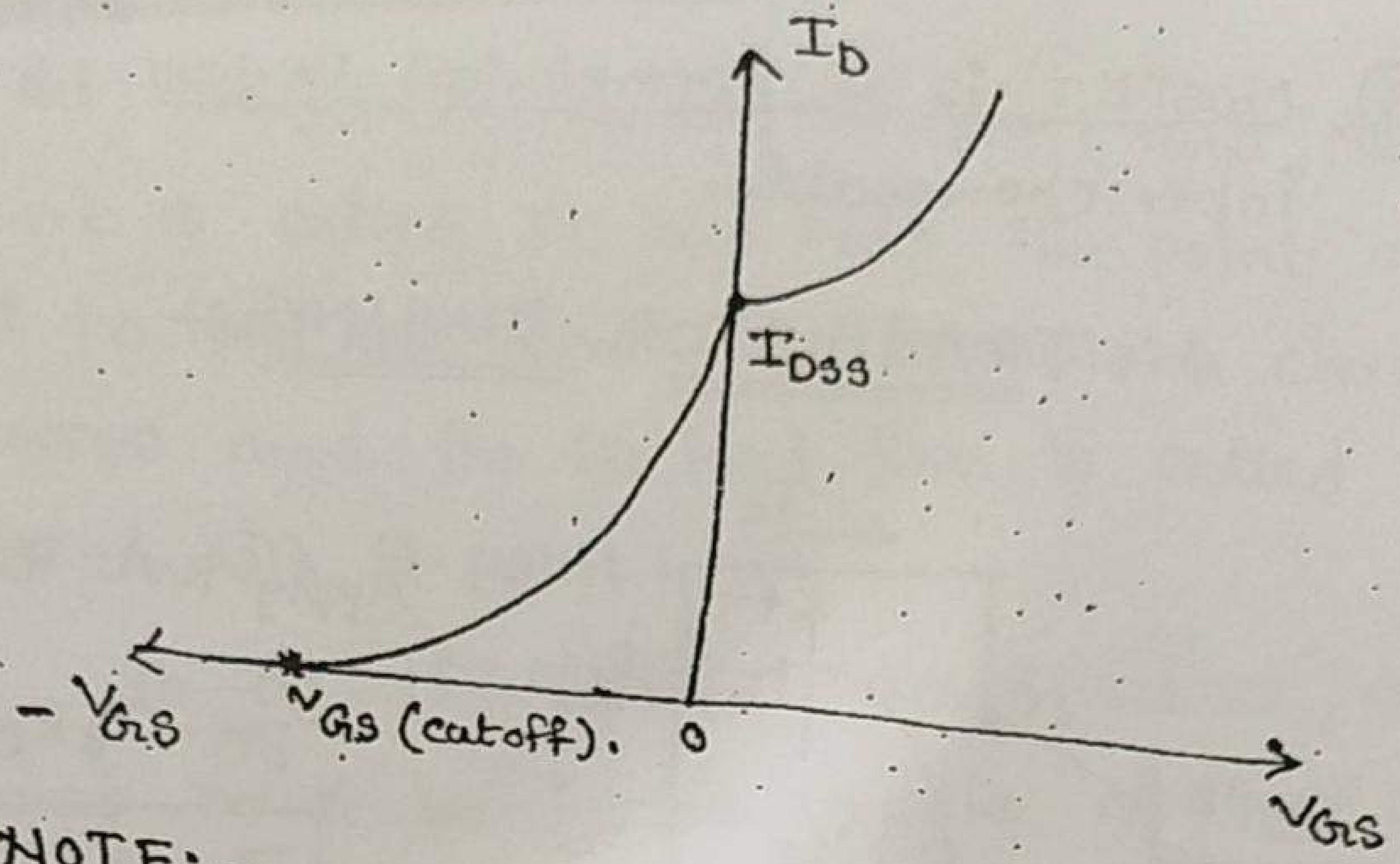
Case (iii):- when $V_{DS} \neq 0$

Drain is higher potential than S. source emits the $\bar{e}$s & drain collects these $\bar{e}$s.

→ when $V_{GS}=0V$ $I_D = I_{DSS}$

As $V_{GS}\uparrow$ (+ve direction) ⇒ $I_D \uparrow$.

$V_{GS}\uparrow$ (-ve direction) ⇒ $I_D \downarrow$.



NOTE:-

① when Gate - O.C :

JFET acts as a LINEAR RESISTOR.
D-MOSFET " " " " .
E-MOSFET " " open switch.

② JFET operated only in ~~Enhancem~~ Depletion mode only
E-MOSFET operated only in Enhancement "
D-MOSFET operated in both the modes.

③ JFET input Resistance is 10^8 to $10^{10}\,\Omega$,
MOSFET input Resistance is 10^{10} to $10^{15}\,\Omega$.

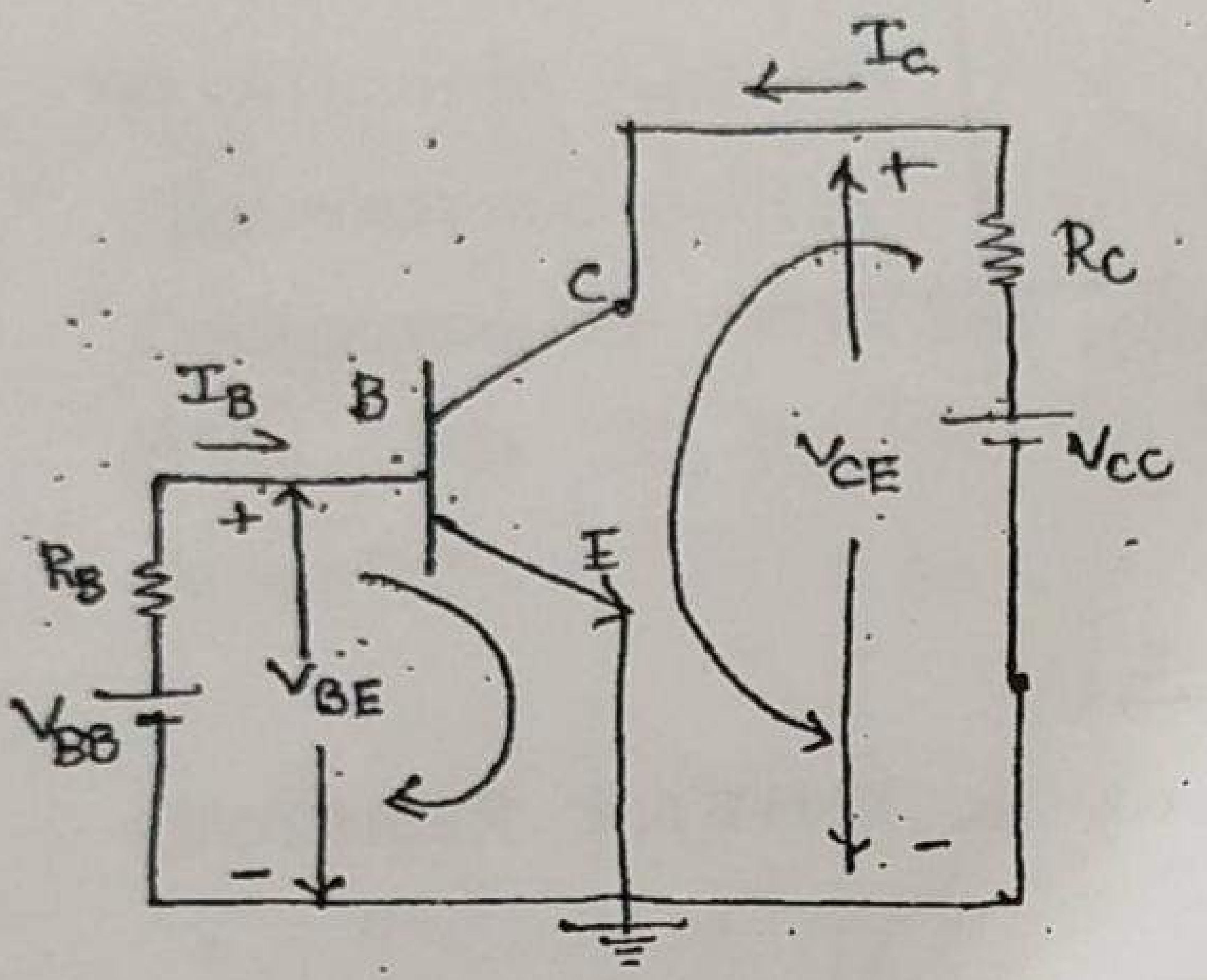
④ Gate current of the JFET in the order of "nano amp".
Gate current of the MOSFET in the order of "pico amp".

⑤ The size of MOSFET smaller than that of JFET.

⑥ The MOSFETS are used in VLSI & VLSI ckts whereas JFETS are restricted to Digital logic ckts.

(7) MOSFET is a symmetrical Device i.e 'S & D' are inter changeable.

TRANSISTOR BIASING:-



Apply KVL to i/p loop

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\boxed{I_B = \left(\frac{V_{BB} - V_{BE}}{R_B}\right)}$$

Apply KVL to o/p loop

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}} \quad \&$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

* on x-axis - y-axis component is '0'

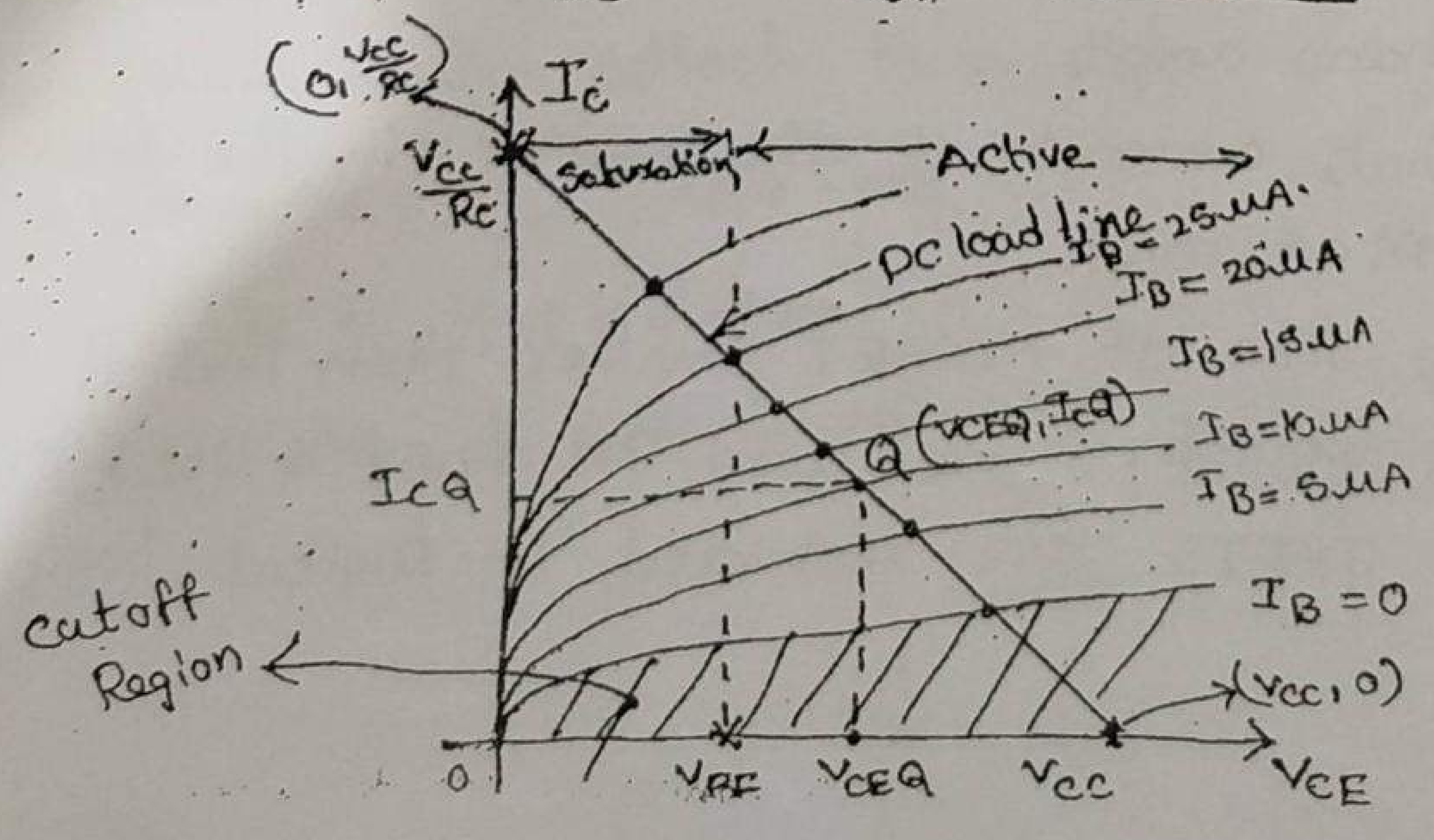
$(I_C = 0)$

$\boxed{V_{CE} = V_{CC}}$ → Max o/p voltage

* on Y-axis - x-axis component is '0'

$(V_{CE} = 0)$

$$I_C = \frac{V_{CC} - \cancel{V_{CE}}^{\,0}}{R_C} = \frac{V_{CC}}{R_C} \Rightarrow \boxed{I_C = \frac{V_{CC}}{R_C}} \rightarrow \text{max o/p current.}$$



The line joining the cut off point and the saturation point is called DC load line. The point of intersection of DC load line and the transistor characteristic curve and the DC load line is called operating point (or) Q. point.

To do the faithful amplification, the operating point must be in the middle of the DC load line (or) near about the middle of the DC load line.

$Q(V_{CE}, I_C)$.

$$I_C = \beta I_B + (1+\beta) I_0.$$

Due to collection of charged particles by 'c' temp across the jn $J_C \uparrow$

As Temp $\uparrow \Rightarrow I_0, \beta$ & V_{BE} varies.

Effect of temp on I_0, β & V_{BE} :-

(i) As $T\uparrow$ $I_0\uparrow$

for every $1^\circ c \uparrow$ temp $I_0 \uparrow$ by 7%.

for every $10^\circ c \uparrow$ " I_0 doubles.

$$\left.\begin{array}{l} T_1{}^\circ c \rightarrow I_{01} \\ T_2{}^\circ c \rightarrow I_{02} \end{array}\right\} \boxed{I_{02} = I_{01} \cdot 2^{\left(\frac{T_2 - T_1}{10}\right)}}$$

(ii) As $T\uparrow$ $\beta\uparrow$.

for $50^\circ c \uparrow$ temp. β value of Ge transistor Doubles.

for $100^\circ c \uparrow$ " " of Si " "

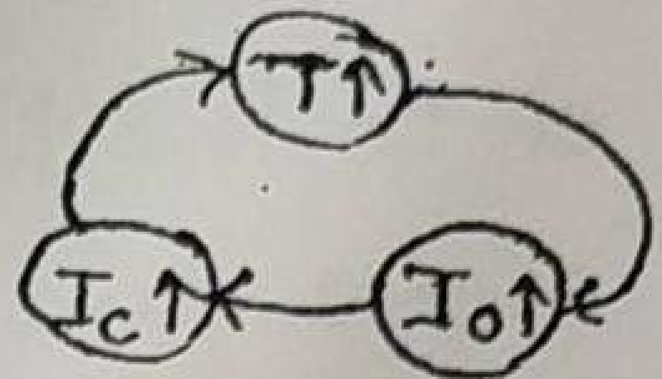
(iii) As $T\uparrow$ $V_{BE}\downarrow$

for $1^\circ c \uparrow$ temp. $V_{BE} \downarrow$ by 2.5mV

"I_c effected more by I_0".

$$\boxed{I_C = f\left[I_0, V_{BE}, \beta\right]}$$

* As $T\uparrow \Rightarrow I_0\uparrow$
As $I_0\uparrow = I_C\uparrow$
As $I_C\uparrow \Rightarrow T\uparrow$



Due to the collection of charged particles by the collector temp across the Junction J_c increases. It becomes accummulative process. At some particular stage the temp across the Junction becomes max and the breakdown of the collector Junction takes place, this process is called "Thermal Runaway". This is due to unstability in the transistor simply the self distruction of an unstabilized transistor is called thermal Runaway. to avoid thermal Runaway the transistor must be stabilised.

Stabilization:-

I_0, V_{BE}, & β due to temp.

The process of making the operating point independent of the variations in I_0, V_{BE}, β due to temp in termed as stabilization.

The process of keeping the operating point in the active region is termed as stabilization.

The stability of a transistor is measured in stability factor.

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stability factor:-

$$I_c = f\,[V_{BE}, I_0, \beta]$$

$$\Delta I_c = \left\{\begin{array}{l}\text{change in } I_c \text{ due} \\ \text{to } I_0 \text{ alone}\end{array}\right\} + \left\{\begin{array}{l}\text{change in } I_c \text{ due} \\ \text{to } V_{BE} \text{ alone}\end{array}\right\} + \left\{\begin{array}{l}\text{change in } I_c \\ \text{to } \beta \text{ alone}\end{array}\right.$$

$$\Delta I_c = \left(\frac{\Delta I_c}{\Delta I_0} \times \Delta I_0\right)\Bigg|_{\substack{V_{BE},\beta \\ = \text{constant}}} + \left(\frac{\Delta I_c}{\Delta V_{BE}} \times \Delta V_{BE}\right)\Bigg|_{\substack{I_0,\beta \\ = \text{constant}}} + \left(\frac{\Delta I_c}{\Delta \beta} \times \Delta\beta\right)\Bigg|_{\substack{I_0,V_{BE} \\ = \text{constant}}}$$

$$\Delta I_c = \frac{\Delta I_c}{\Delta I_0}\Bigg|_{\substack{V_{BE},\beta \\ \text{constant}}} \times \Delta I_0 + \frac{\Delta I_c}{\Delta V_{BE}}\Bigg|_{\substack{I_0,\beta \\ \text{constant}}} \Delta V_{BE} + \frac{\Delta I_c}{\Delta \beta}\Bigg|_{\substack{I_0,V_{BE} \\ \text{constant}}} \Delta\beta$$

$$\boxed{\Delta I_c = S \cdot \Delta I_0 + S' \Delta V_{BE} + S'' \Delta\beta}$$

where
$$\left.\begin{array}{l} S = \dfrac{\Delta I_c}{\Delta I_0}\Bigg|_{V_{BE},\beta = \text{constant}} \\ S' = \dfrac{\Delta I_c}{\Delta V_{BE}}\Bigg|_{I_0,\beta = \text{constant}} \\ S'' = \dfrac{\Delta I_c}{\Delta \beta}\Bigg|_{I_0,V_{BE} = \text{constant}} \end{array}\right\} \text{stability factor.}$$

stability factor (S) :-

$$S = \frac{\Delta I_c}{\Delta I_0} \text{ (or) } \frac{dI_c}{dI_0}\Bigg|_{V_{BE},\beta = \text{constant}}$$

$$I_c = \beta I_B + (1+\beta) I_0$$

Diff w.r.t I_c

$$1 = \beta \frac{dI_B}{dI_c} + (1+\beta)\frac{dI_0}{dI_c}$$

$$1-\beta\frac{dI_B}{dI_C} = (1+\beta)\cdot\frac{1}{S}$$

$$\boxed{S = \frac{(1+\beta)}{1-\beta\frac{dI_B}{dI_C}}}$$

To calculate $\frac{dI_B}{dI_C}$,

(i) always take i/p loop eq. of the given transistor ckt.

(ii) Diff w.r.t I_C

we get $\left(\frac{dI_B}{dI_C}\right)$ value.

If $S \rightarrow$ very high (or) high $\left.\right\}$ $S = \frac{\Delta I_C}{\Delta I_0} \rightarrow$ The ckt is thermally LESS stable.

If $S \rightarrow$ low $\Rightarrow$ The ckt is thermally more stable.

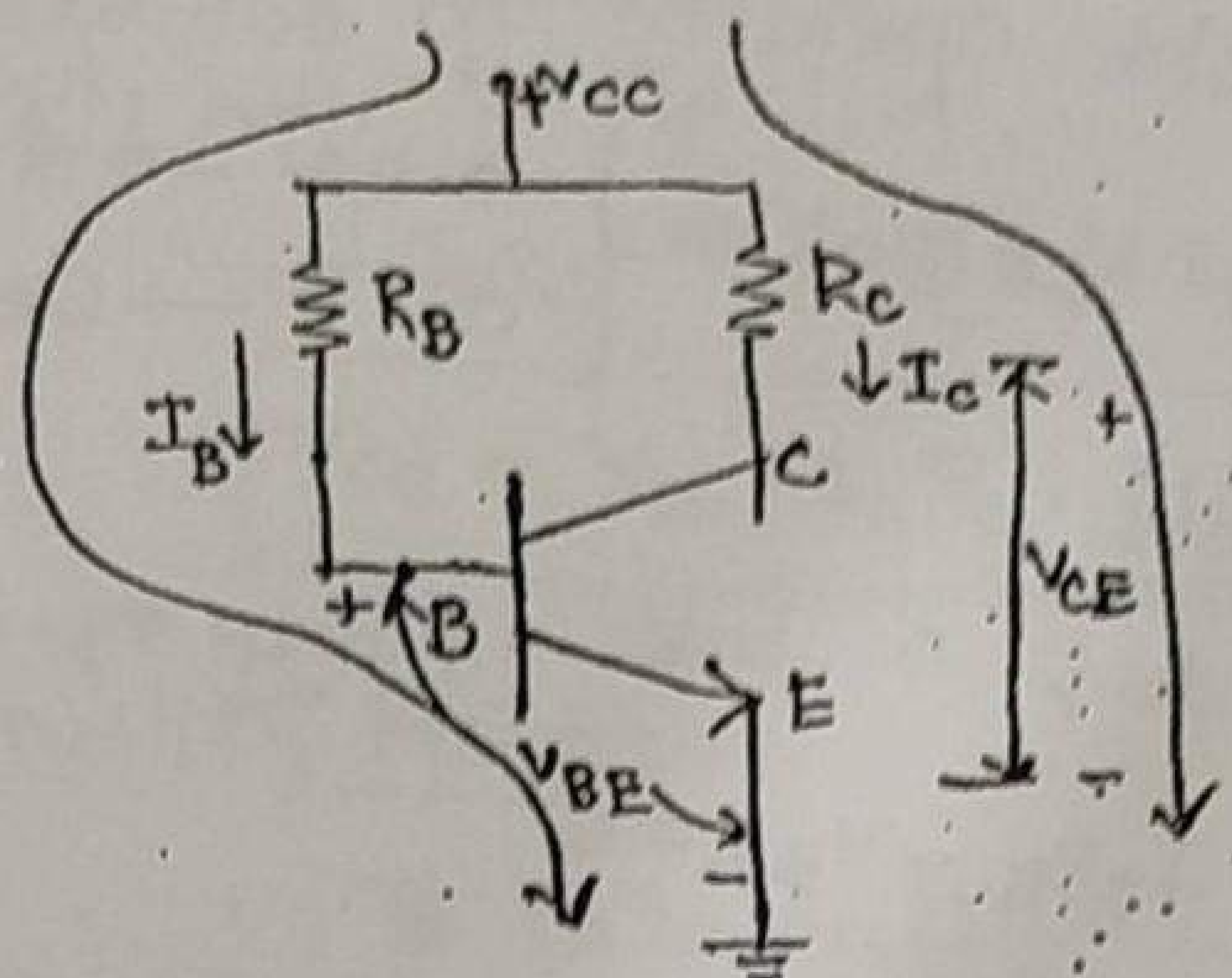
Biasing Methods:-

The biasing methos are used to keep the operating point in the active region.

The Biasing Methods are

1. fixed bias method.
2. collector - to - Base bias (OR) feedback Resistor bias.
3. voltage Divider bias (or) Emitter bias (or) self bias method.

① Fixed bias method :-



Apply KVL to i/p loop :-

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$-I_B = \frac{+V_{BE} - V_{CC}}{R_B} \Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$

$\boxed{I_C = \beta I_B}$ → Assuming the transistor operated in Active region.

Apply KVL to o/p loop :-

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

NOTE :-

If the estimated V_{CE} voltage satisfies the condition.

$$\boxed{V_{CE(sat)} < V_{CE} < V_{CC}}$$

→ Transistor operated in Active Region.

(OR)

$V_{BE} = V_\gamma \longrightarrow J_E - F.B$ } Active Region

$V_{CE} > V_R \longrightarrow J_C - R.B$

Else the transistor operated in saturation Region.

If the transistor operated in saturation Region

$$-V_{CE} = V_{CE(sat)} = \begin{cases} 0.2V \rightarrow Si. \\ 0.1V \rightarrow Ge. \end{cases}$$

Stability factor:-

To calculate S take i/p loop eq.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Diff w.r.t I_C

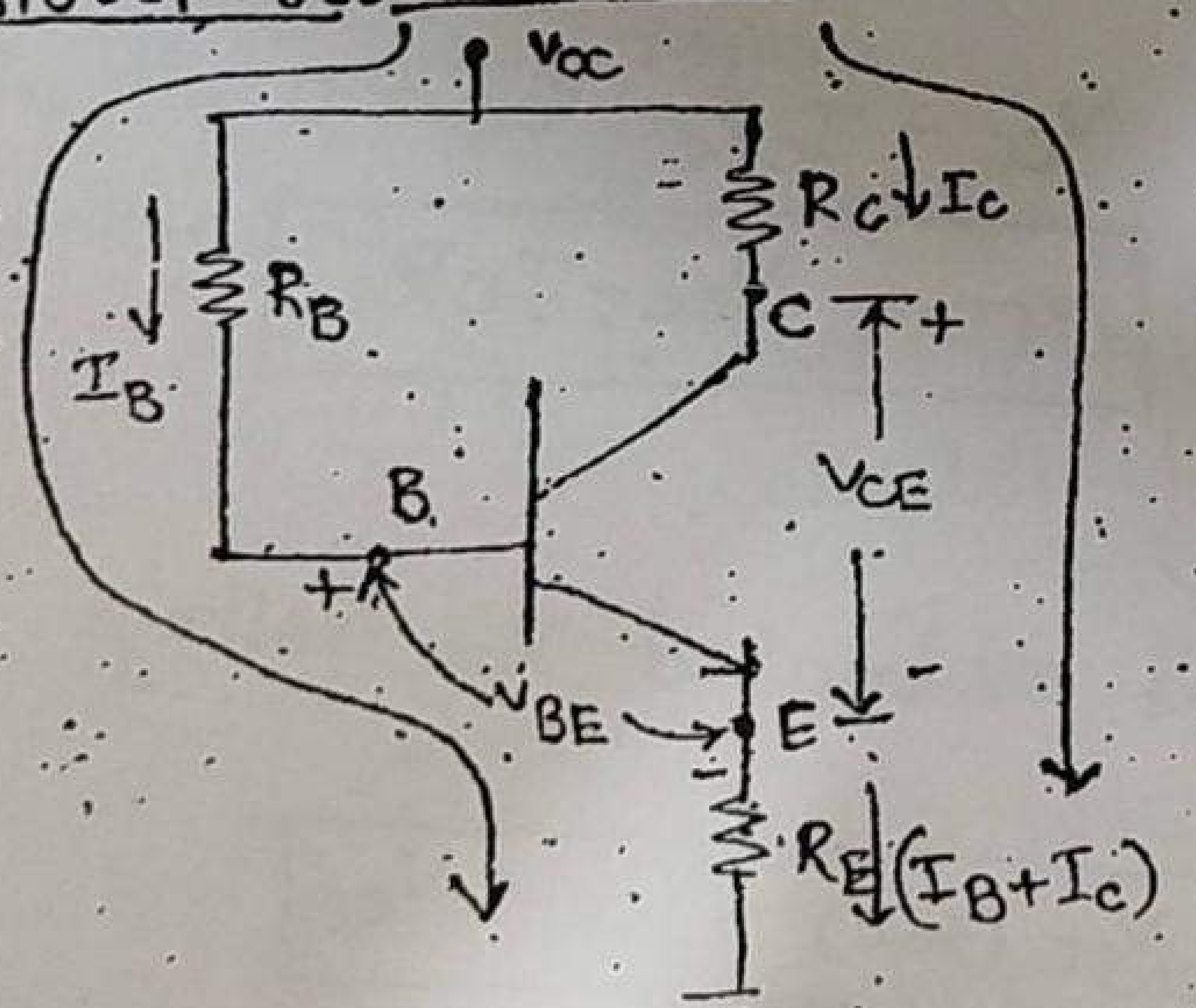
$$0 - \frac{dI_B}{dI_C} \times R_B - 0 = 0$$

$$\therefore \frac{dI_B}{dI_C} = 0$$

$\boxed{S = (1+\beta)}$ $\beta \rightarrow$ high, $S \rightarrow$ high

* The fixed bias ckt is thermally less stable.

* To increase the thermal stability of this ckt connect a Resistor at emitter.



Apply KVL to i/p loop

$$V_{CC} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0$$

$$\boxed{I_C = \beta I_B}$$

$\downarrow$

Assuming the transistor in the Active region.

$$\boxed{(I_C + I_B) = (1+\beta) I_B}$$

$$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}}$$

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$$\boxed{I_C = \beta I_B}$$

Apply KVL to o/p loop,

$$V_{CC} - I_C R_C - V_{CE} - (I_C + I_B) R_E = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C - (I_C + I_B) R_E}$$

Stability factor:-

To calculate S, take i/p loop eqn,

$$V_{CC} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0$$

$$V_{CC} - V_{BE} - (R_B + R_E) I_B - I_C R_E = 0$$

Diff w.r.t I_C

$$0 - 0 - (R_B + R_E) \frac{dI_B}{dI_C} - R_E = 0$$

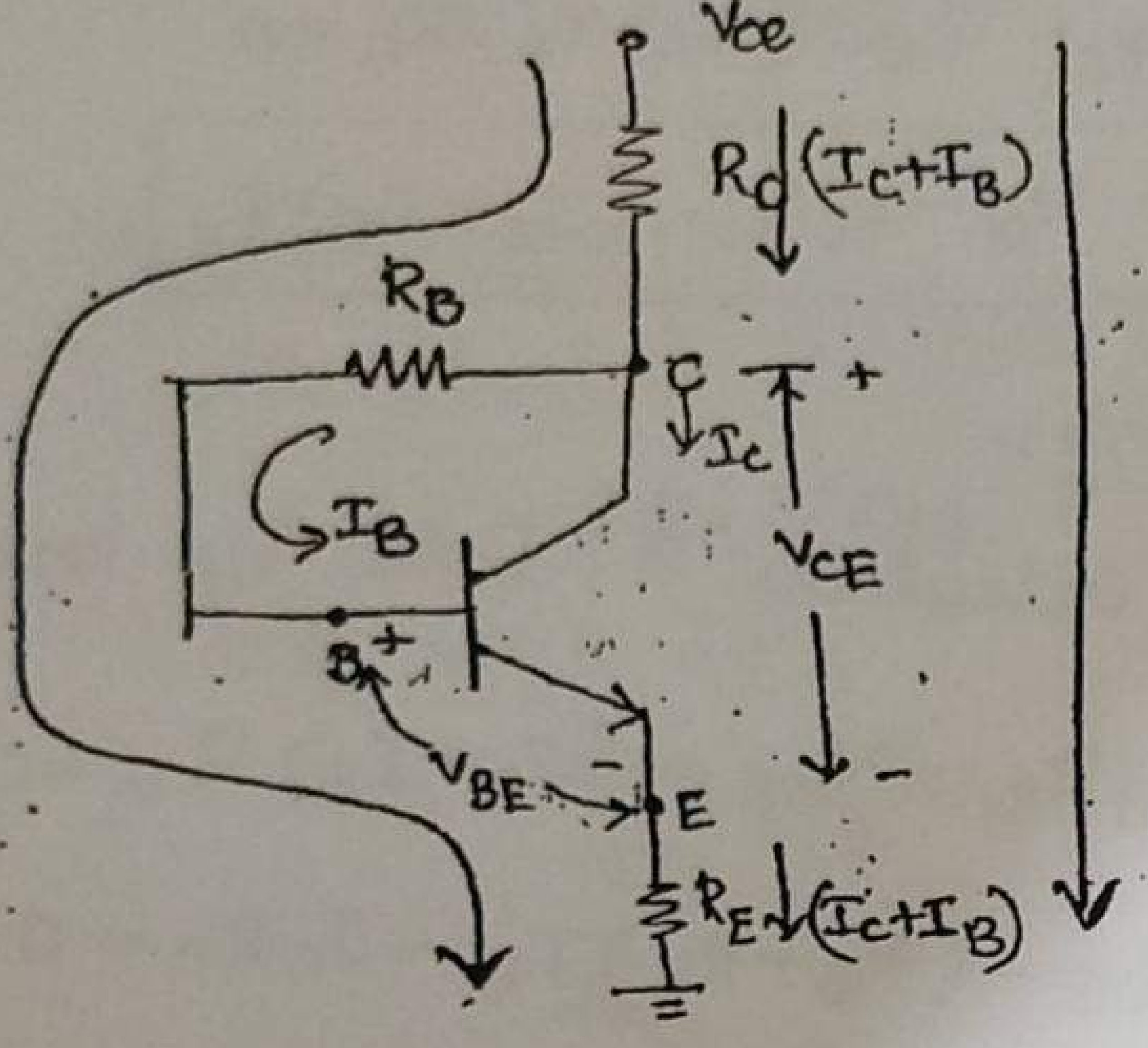
$$\frac{dI_B}{dI_C} = -\left(\frac{R_E}{R_B + R_E}\right)$$

$$\boxed{S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B + R_E}\right)}}$$

As $D_r > 1$, $S < (1+\beta)$.

The fixed bias ckt with R_E is thermally more stable compared to without R_E ckt.

2. collector - to-Base bias (or) feed back Resistor bias method :-



Apply KVL to i/p loop

$$V_{CC}-(I_C+I_B)R_C-I_BR_B-V_{BE}-(I_C+I_B)R_E=0$$

Assume that the transistor operated in the Active region

$$\boxed{I_C=\beta I_B}$$

$$I_C+I_B=(1+\beta)I_B$$

$$V_{CC}-(1+\beta)I_B\cdot R_C-I_BR_B-V_{BE}-(1+\beta)I_BR_E=0$$

$$\boxed{I_B=\frac{V_{CC}-V_{BE}}{R_B+(1+\beta)(R_C+R_E)}}$$

$$\boxed{I_C=\beta I_B}$$

Apply KVL to o/p loop

$$V_{CC}-(I_C+I_B)R_C-V_{CE}-(I_C+I_B)R_E=0$$

$$\boxed{V_{CE}=V_{CC}-(I_C+I_B)(R_C+R_E)}$$

Stability factor (S) :-

To calculate S take i/p loop eq.

$$V_{CC}-(I_C+I_B)R_C-I_BR_B-V_{BE}-(I_C+I_B)R_E=0$$

$$V_{CC}-V_{BE}-(R_C+R_B+R_E)I_B-(R_C+R_E)I_C=0$$

Diff w.r.t I_C

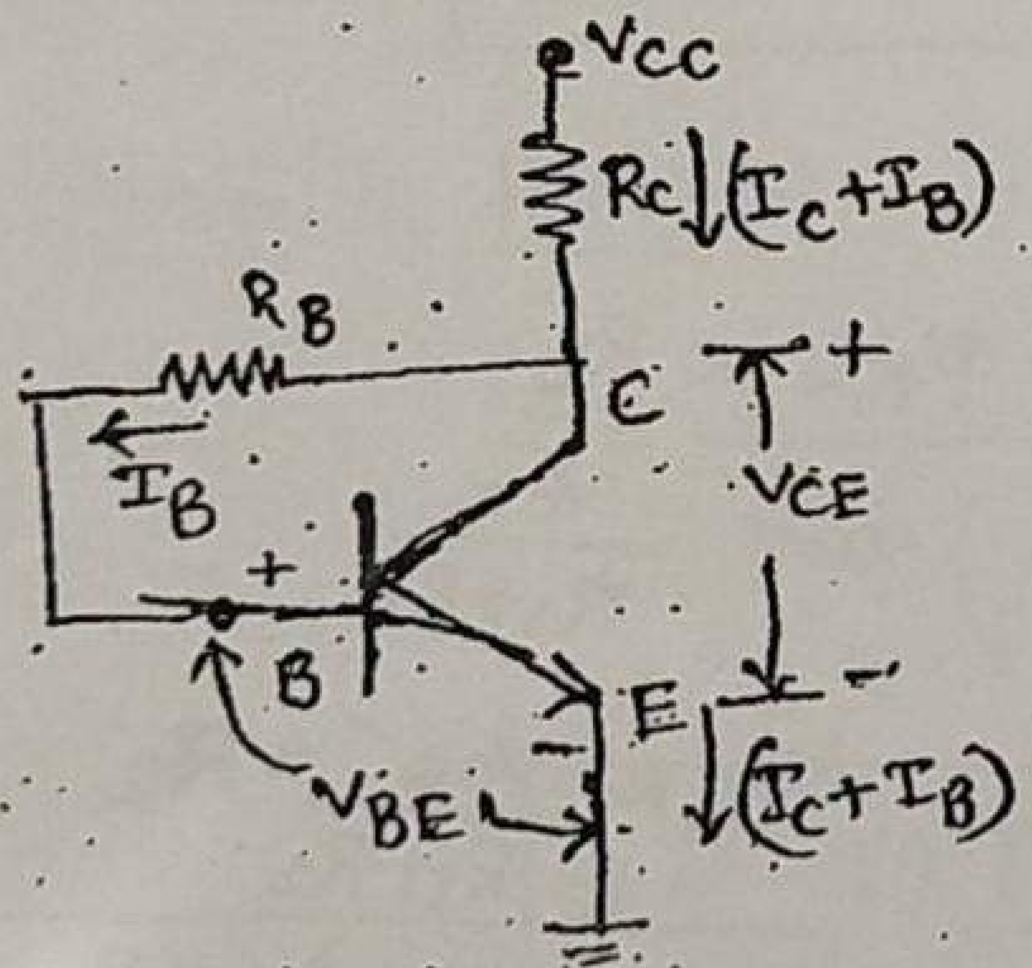
$$0 - 0 - (R_C + R_B + R_E)\frac{dI_B}{dI_C} - (R_C + R_E) = 0$$

$$\boxed{\frac{dI_B}{dI_C} = -\left[\frac{R_C + R_E}{R_C + R_B + R_E}\right]}$$

$$* \boxed{S = \frac{1+\beta}{1+\beta\left(\frac{R_C + R_E}{R_C + R_B + R_E}\right)}}$$

$$S = \frac{(1+\beta)}{1+\beta\left[\frac{(I_C + I_B)\text{ current flowing resistors sum}}{I_B\text{ current flowing resistor sum}}\right]}$$

<u>without</u> <u>Re</u>:-



Put $R_E = 0$.

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C}}$$

$$I_C = \beta I_B.$$

$$\boxed{V_{CE} = V_{CC} - (I_C + I_B)R_C}$$

$$\boxed{S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)}}$$

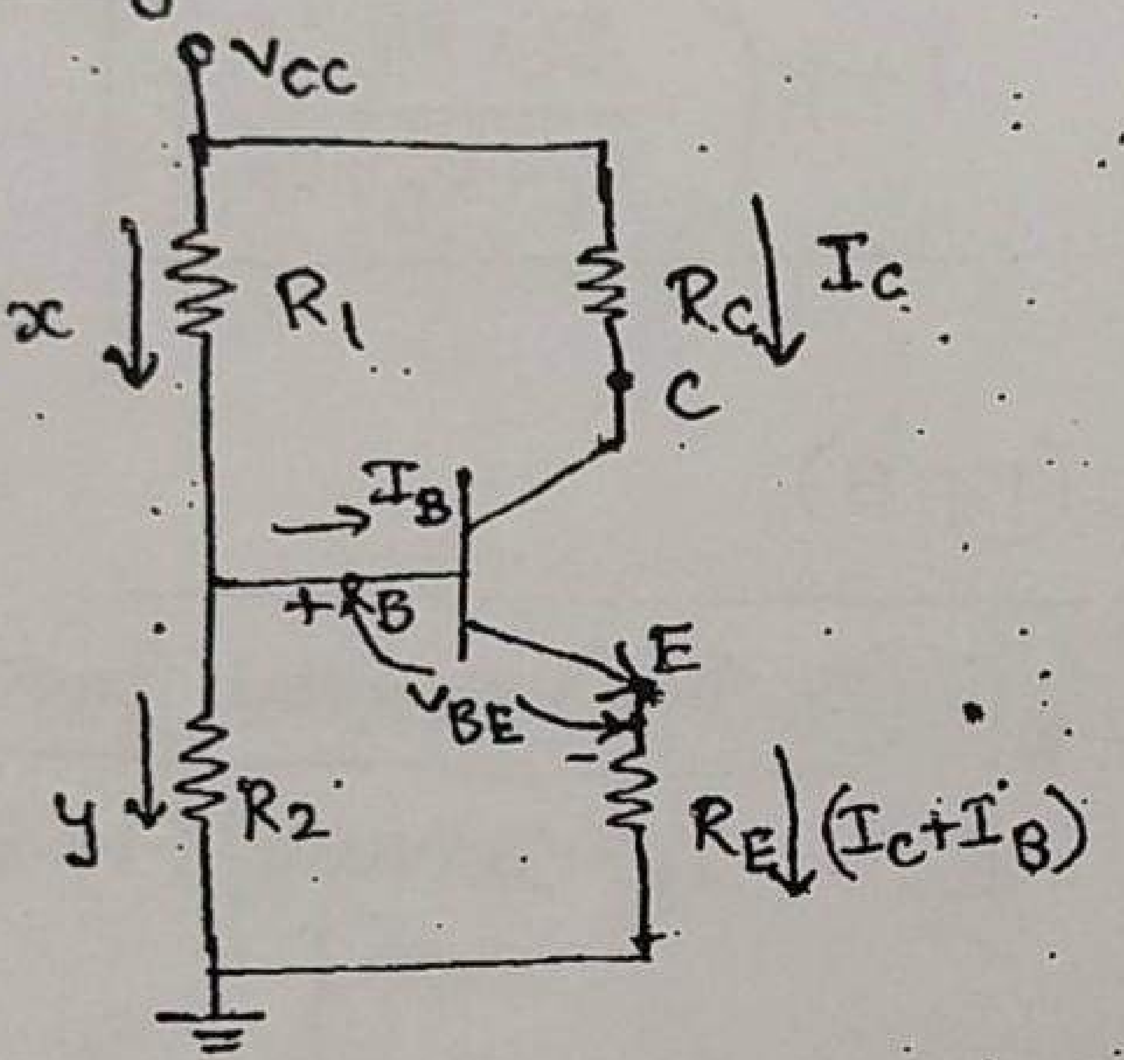
* collector to base bias ckt is thermally more stable compared to fixed bias ckt.

$$S = \frac{(1+\beta)}{1+\beta\left[\frac{R_C}{R_C+R_B}\right]} \qquad \text{If } R_C \simeq 0 \quad \boxed{S \simeq 1+\beta}$$

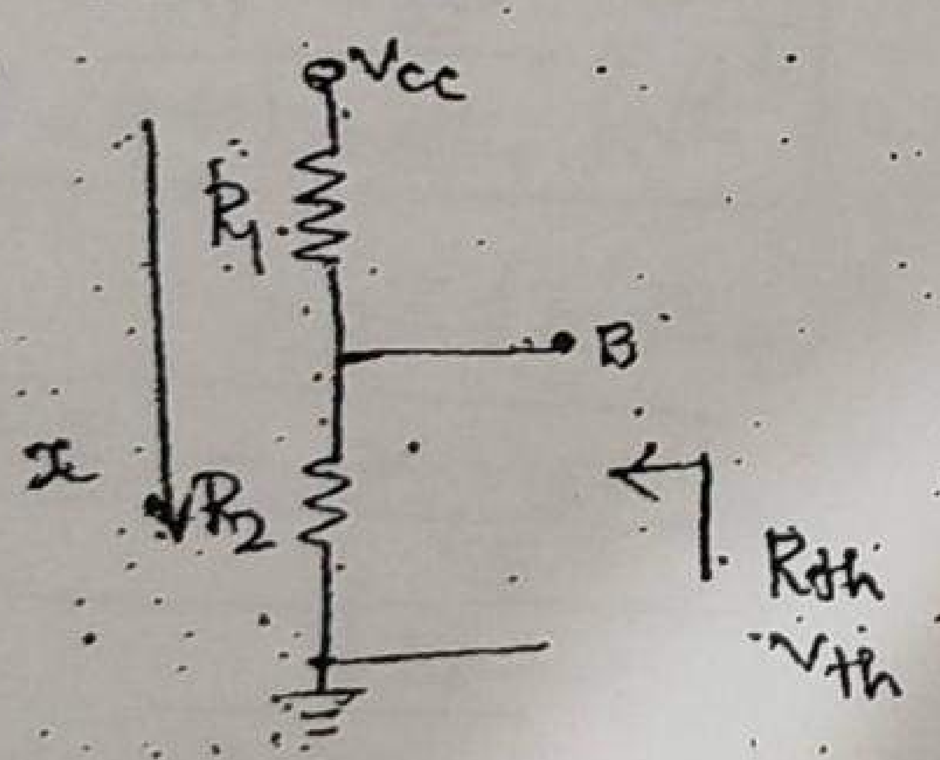
The ckt is thermally less stable.

∴ For collector to Base bias method 'R_C' value Should NOT very small.

3. Voltage Divider (or) Emitter (or) self bias method:-



Thevenin's eq ckt:-



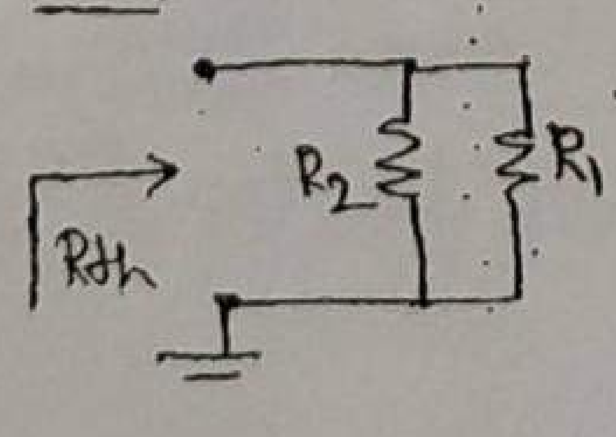
$$V_{th} = x\,R_2$$

$$x = \frac{V_{cc}}{R_1+R_2}$$

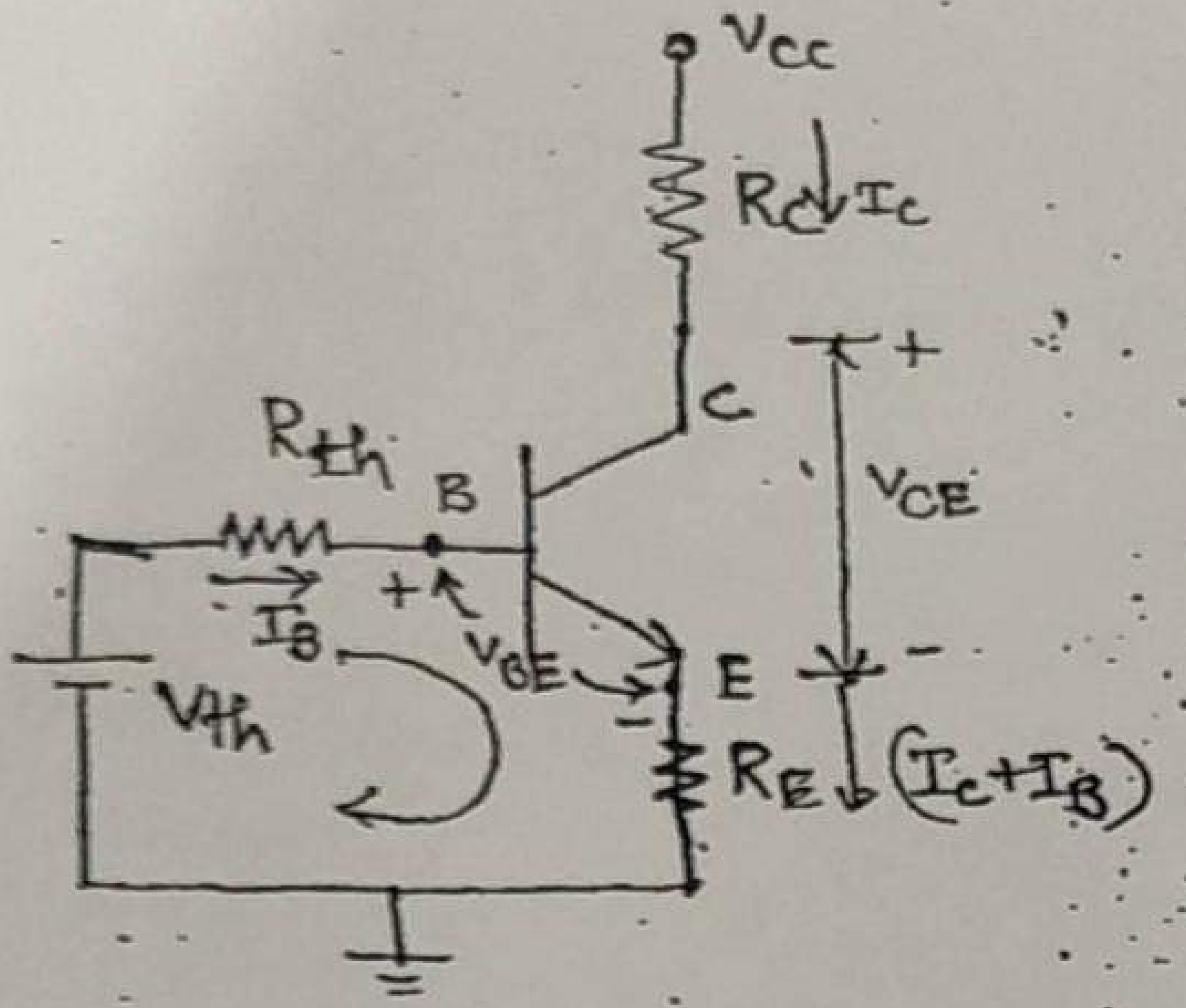
$$V_{th} = \frac{V_{cc}}{R_1+R_2} \times R_2$$

$$\boxed{V_{th} = V_{cc}\left(\frac{R_2}{R_2+R_1}\right)}$$

R_{th}:-



$$\boxed{R_{th} = \frac{R_1 R_2}{R_1+R_2}}$$



Apply KVL to i/p loop:-

$$V_{th} - I_B R_{th} - V_{BE} - (I_C+I_B)R_E =$$

Assume that the transistor operated in the Active Region.

$I_C = \beta I_B$ & $(I_C+I_B) = (1+\beta$

$$\Rightarrow V_{th} - V_{BE} - I_B R_{th} - (1+\beta) I_B R_E = 0$$

$$\boxed{I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta) R_E}} \quad \& \quad \boxed{I_C = \beta I_B}$$

Apply KVL to o/p loop:-

$$V_{CC} - I_C R_C - V_{CE} - R_E(I_C + I_B) = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C - (I_C + I_B) R_E}$$

Stability factor:-

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_{th}+R_E}\right)}$$

$$\boxed{S = \frac{1+\beta}{1+\beta\left(\frac{1}{\frac{R_{th}}{R_E}+1}\right)}}$$

if $\frac{R_{th}}{R_E} \rightarrow \infty \Rightarrow S \rightarrow (1+\beta)$

$\therefore$ The ckt is thermally less stable.

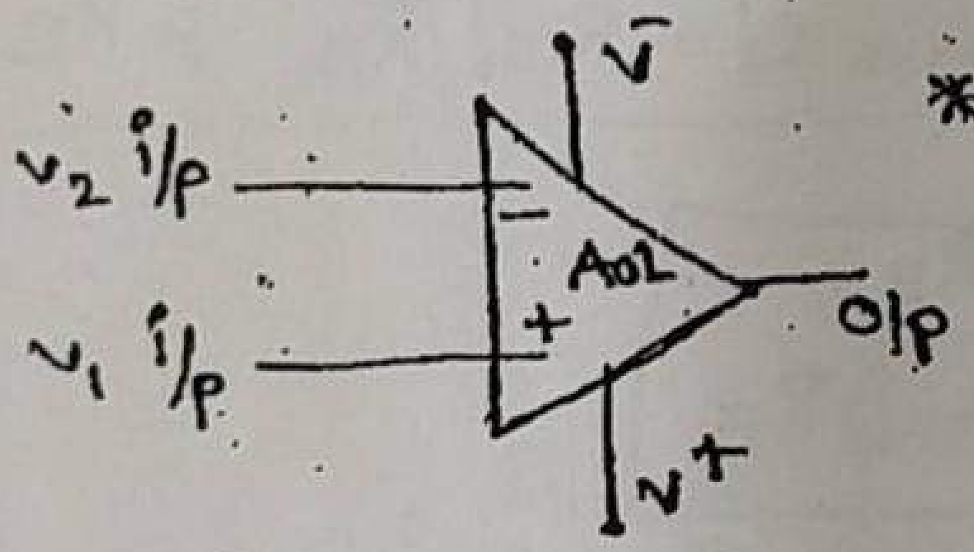
11/11/12

Operational Amplifiers:-

Op. Amp characteristics: — **Ideal char:**

1. input resistance → very high → $R_i = \infty$.
2. output resistance → very low → $R_o \approx 0$..
3. openloop gain (AoL) → very high → $A_{OL} = \infty$.
4. Band width → very high → $BW = \infty$.
5. offset voltages → very low → offset voltages $= 0$
6. Common Mode Rejection Ratio → very high → $CMRR = \infty$
7. Slew Rate → very high → $SR = \infty$

$$SR = \left.\frac{dv_o}{dt}\right|_{max}$$

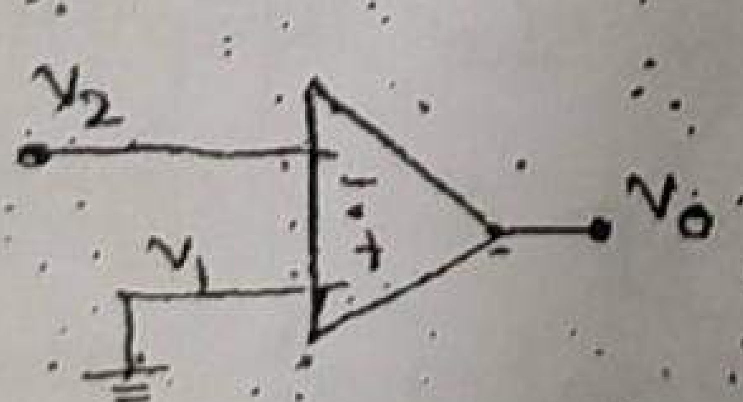


* A Basic op-amp consists minimum of 5 terminals.
  1. 2 i/p terminals
  2. 1 o/p "
  3. 2 supply voltages. (v^+, v^-)
* Remaining terminals depends on its application.

$$* \; V_o = A_{OL}\underbrace{(v_1 - v_2)}_{v_d} \rightarrow \text{Differential i/p voltage}$$

$$\boxed{V_o = A_{OL} \, v_d}$$

when $v_1 = 0$



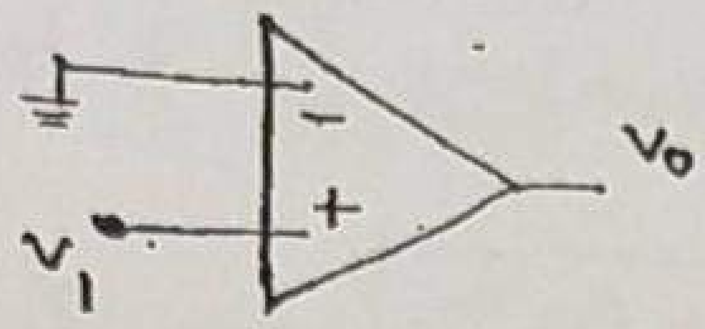
where v_2 = Inverting terminal voltage. $\boxed{\text{Gain -ve}}$

$$v_o = A_{OL}(0 - v_2)$$

$$v_o = -A_{OL}v_2$$

↑ 180° of phase shift b/w v_{in} & v_o.

when $V_2 = 0$:



* +ve sign represents 0° of phase b/w V_0 & V_1.

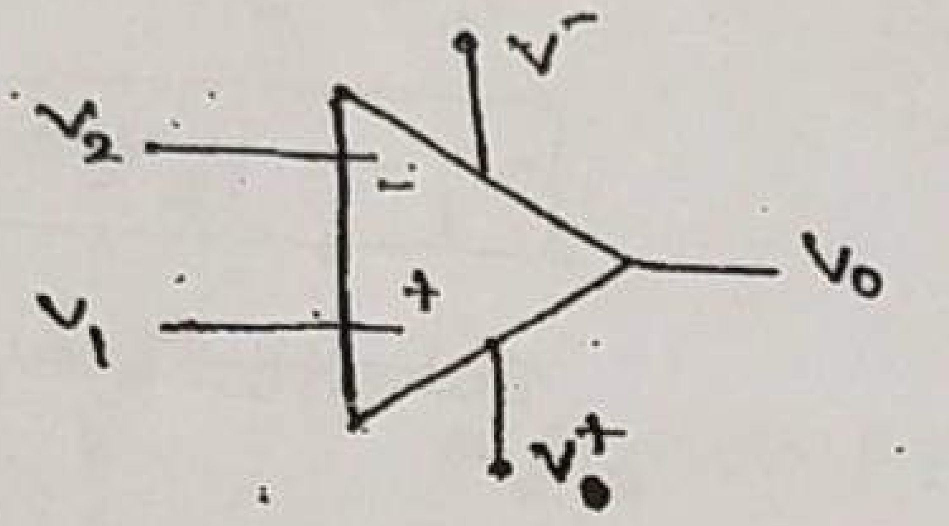
$V_1 \rightarrow$ non inverting terminal voltage

(Gain +ve)

$V_0 = A_{OL}(V_1 - 0)$

$$\boxed{V_0 = A_{OL} V_1}$$

*



$V_0 = A_{OL}(V_1 - V_2)$

$V_0 = A_{OL}(V_d)$

* $\boxed{A_{OL} = \frac{V_0}{V_d}}$

→ for an op-amp A_{OL} is very high, to get this $V_d = 0$ (very low).

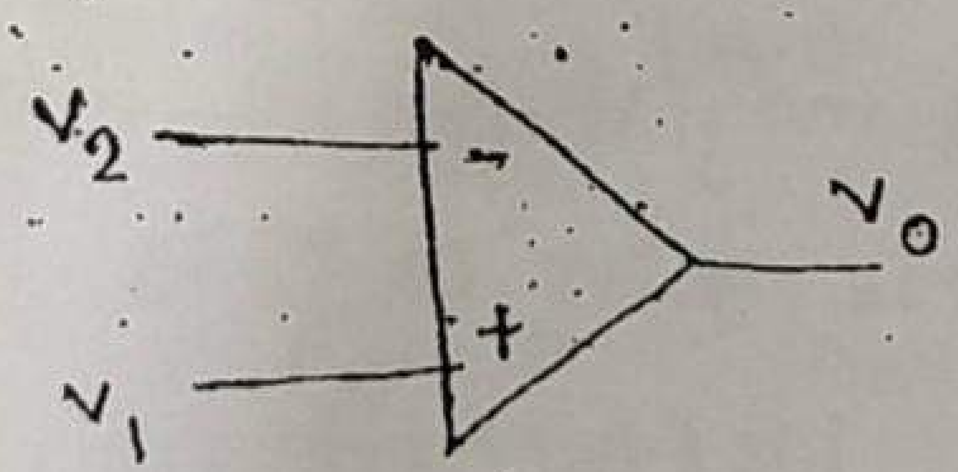
$\boxed{V_0 = A_{OL} V_d} \rightarrow$ Finite value

→ for an ideal op-amp $A_{OL} = \infty$

— To get this value $\underline{V_d = 0}$

$\underline{V_0 = A_{OL} V_d = 0}$

→ But practically the o/p of the op-amp is not equal to zero. So that the output of the op-amp not only depends on the differential i/p voltage But also depends on common mode (Avg signal).



V_1 = Non inverting terminal voltage.

V_2 = Inverting terminal voltage

A_1 = Gain due to V_1 alone.

A_2 = Gain due to V_2 alone.

$V_d = (V_1 - V_2) \rightarrow$ Differential i/p voltage.

$V_c = \left(\frac{V_1+V_2}{2}\right) \rightarrow$ common mode voltage.

Total o/p voltage $(V_0) = \begin{Bmatrix} \text{o/p voltage due} \\ \text{to } V_1 \text{ alone} \end{Bmatrix} + \begin{Bmatrix} \text{o/p voltage due} \\ \text{to } V_2 \text{ alone} \end{Bmatrix}$

$$\boxed{V_0 = A_1V_1 + A_2V_2} \longrightarrow ①$$

we know that

$V_d = V_1 - V_2$

$\therefore \boxed{V_1 = V_d + V_2}$

$V_c = \frac{V_1+V_2}{2}$

$= \frac{V_d+V_2+V_2}{2}$

$V_c = \frac{1}{2}V_d + V_2$

$$\boxed{\therefore V_2 = -\tfrac{1}{2}V_d + V_c} \longrightarrow ②$$

; $V_1 = V_d + V_2$

$V_1 = V_d + -\tfrac{1}{2}V_d + V_c$

$$\boxed{V_1 = \tfrac{1}{2}V_d + V_c} \longrightarrow ③$$

~~Substitute V_1 & V_2~~ in eq ①

substitute ② & ③ in eq ①

$$V_0 = A_1\left(\tfrac{1}{2}V_d + V_c\right) + A_2\left(-\tfrac{1}{2}V_d + V_c\right)$$

$$= \left(\frac{A_1 - A_2}{2}\right)V_d + (A_1 + A_2)V_c$$

$$\boxed{V_0 = A_dV_d + A_cV_c}$$

$A_d \rightarrow$ Differential mode voltage gain

$A_c \rightarrow$ common " " "

Common Mode Rejection Ratio :-

It is a Ratio of magnitudes of differential mode gain to common mode gain so it is

$$CMRR = \left|\frac{A_d}{A_c}\right| = \left|\frac{\tfrac{1}{2}(A_1 - A_2)}{A_1 + A_2}\right| = \frac{1}{2}\left|\frac{A_1 - A_2}{A_1 + A_2}\right|$$

always $A_1 \rightarrow +ve$

$A_2 \rightarrow -ve$

$A_d \ggg A_c$ so $\boxed{CMRR \rightarrow \text{very high value}}$

for a general purpose op-amp, $CMRR \rightarrow 140dB$.

$$(CMRR)_{dB} = 20\log_{10}\left|\frac{A_d}{A_c}\right| = 140dB$$

$$\log_{10}\left|\frac{A_d}{A_c}\right| = 7dB.$$

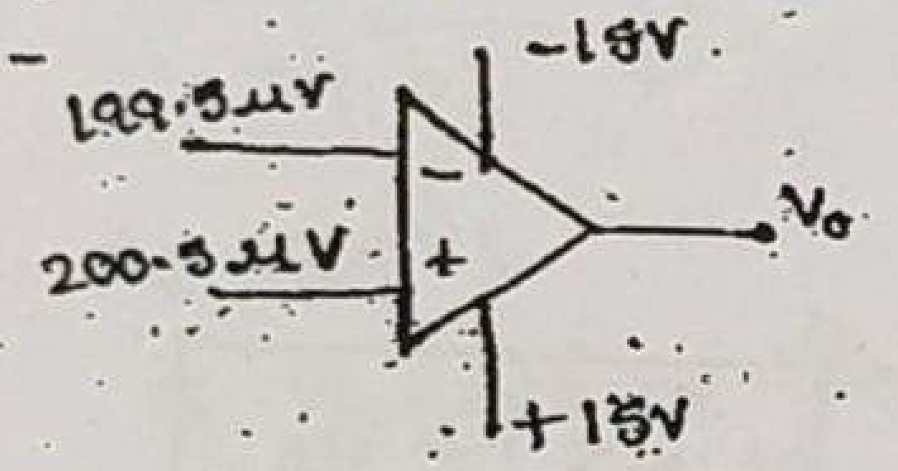
$$\left|\frac{A_d}{A_c}\right| = 10^7 dB.$$

$$A_dV_d \ggg A_cV_c$$

$\boxed{\therefore V_0 \simeq A_dV_d}$ ∴ The o/p of the op-amp mainly depends on V_d.

* The op-amp works on the principle of $V_d \simeq 0$.

Ex:-



* for the op-amp shown CMRR is 140dB & $A_c = 1$ calculate the total o/p voltage.?

$$\boxed{V_0 = A_dV_d + A_cV_c}$$

$$V_d = (V_1 - V_2) = 1\mu V$$

$$V_c = \frac{199.5 + 200.5}{2} = 200\mu V$$

$$CMRR = 140dB$$

$$20\log\left|\frac{A_d}{A_c}\right| = 140$$

$$\frac{A_d}{A_c} = 10^7 \qquad A_c = 1$$

$$\boxed{A_d = 10^7}$$

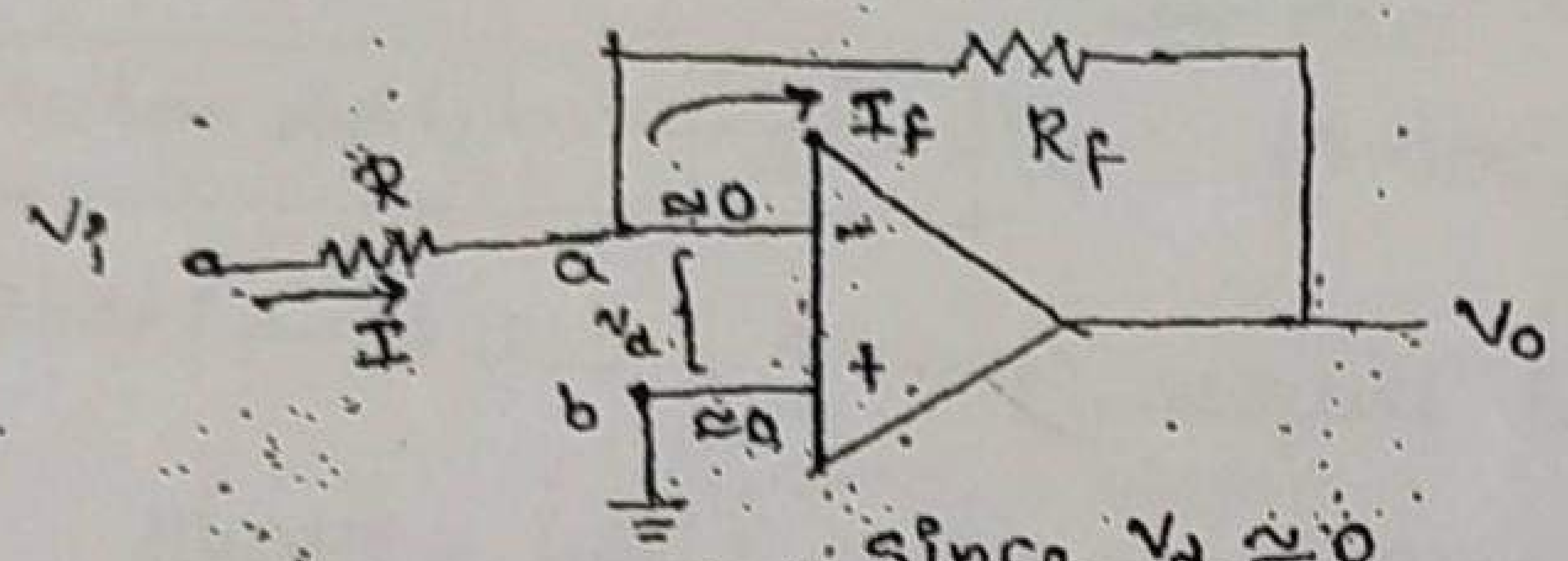
$$\therefore V_0 = 10^7 \times 10^{-6} + 1 \times 200 \times 10^{-6}$$

$$= 10 + 0.0002$$

$$\therefore \boxed{V_0 = 10.0002V}$$

Negative feedback applications:- (Linear type).

1. INVERTING Amplifier:-



Since $v_d \simeq 0$

$\therefore (v_b - v_a) \simeq 0$

$\boxed{v_b \simeq v_a}$

But $v_b = 0$, $v_a \simeq 0$.

→ So the Node 'a' called as "VIRTUAL GROUND"

→ The input resistance of the op-amp is very high. The current entering into the op-amp terminals is very low ($\simeq 0$).

$\therefore$ Apply KCL at 'a'.

$$I = I_f$$

$$\frac{v_i - \cancel{v_a}^{0}}{R} = \frac{\cancel{v_a}^{0} - v_o}{R_f}$$

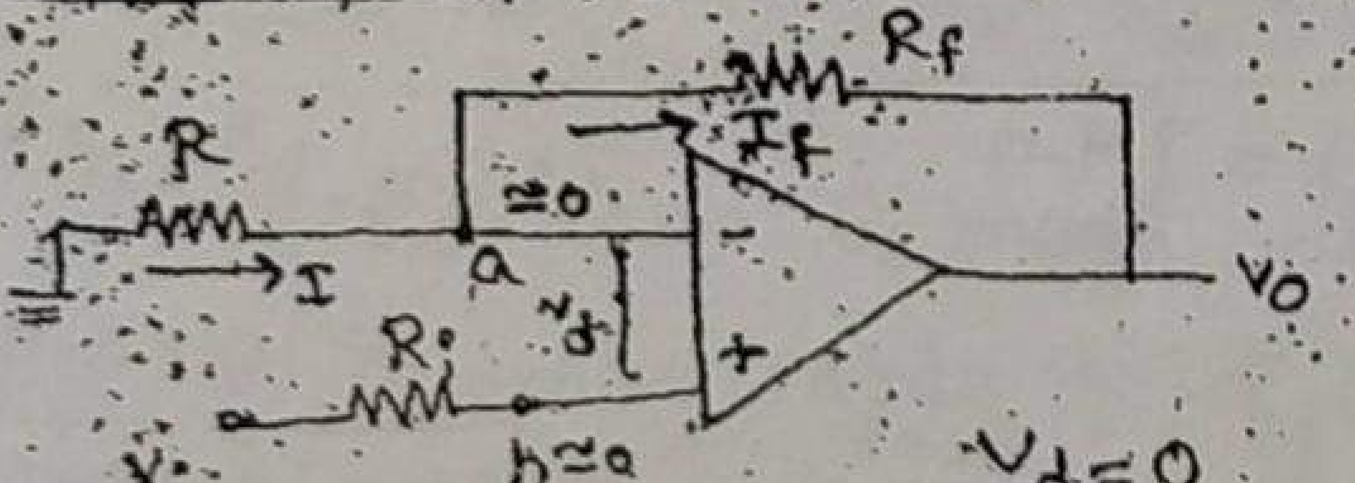
$$\frac{v_i}{R} = \frac{-v_o}{R_f}$$

$$\boxed{v_o = -\frac{R_f}{R} v_i}$$

180° of phase shift b/w v_o & v_i.

→ Gain $= \frac{v_o}{v_i} = \frac{-R_f/R \, v_i}{v_i} = \frac{-R_f}{R}$.

2. Non-inverting Amp:-



$v_d \simeq 0$

$\boxed{v_b \simeq v_a}$

But $v_b \simeq v_i$ $\boxed{v_a \simeq v_i}$

Apply KCL at 'a'.

$$I = I_f$$

$$\frac{0 - V_a}{R} = \frac{V_a - V_o}{R_f}$$

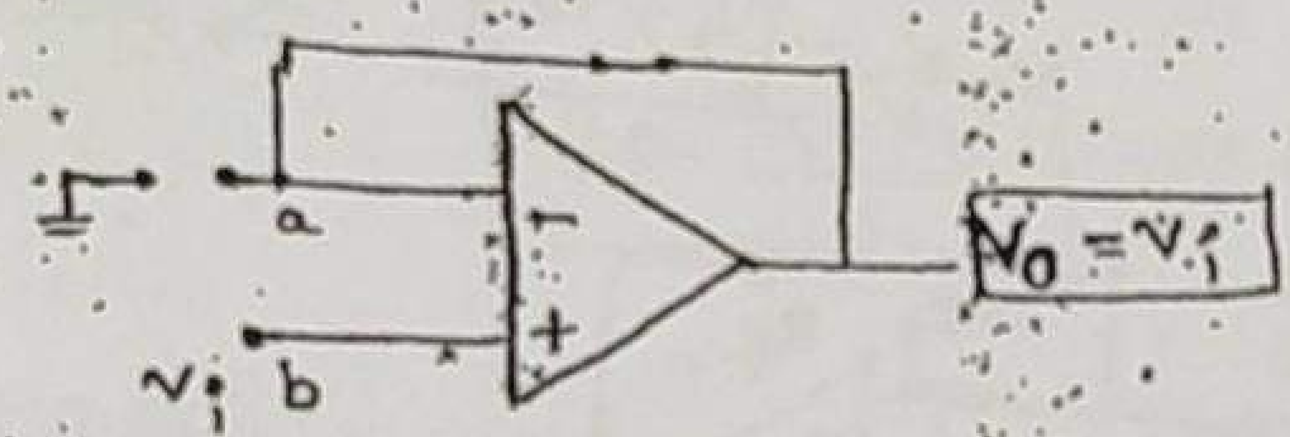
$$-\frac{R_f}{R} V_a = V_a - V_o$$

$$V_o = V_a\left(1 + \frac{R_f}{R}\right)$$

$$\boxed{V_o = V_i\left(1 + \frac{R_f}{R}\right)}$$

→ Gain $= \frac{V_o}{V_i} = \left(1 + \frac{R_f}{R}\right)$.

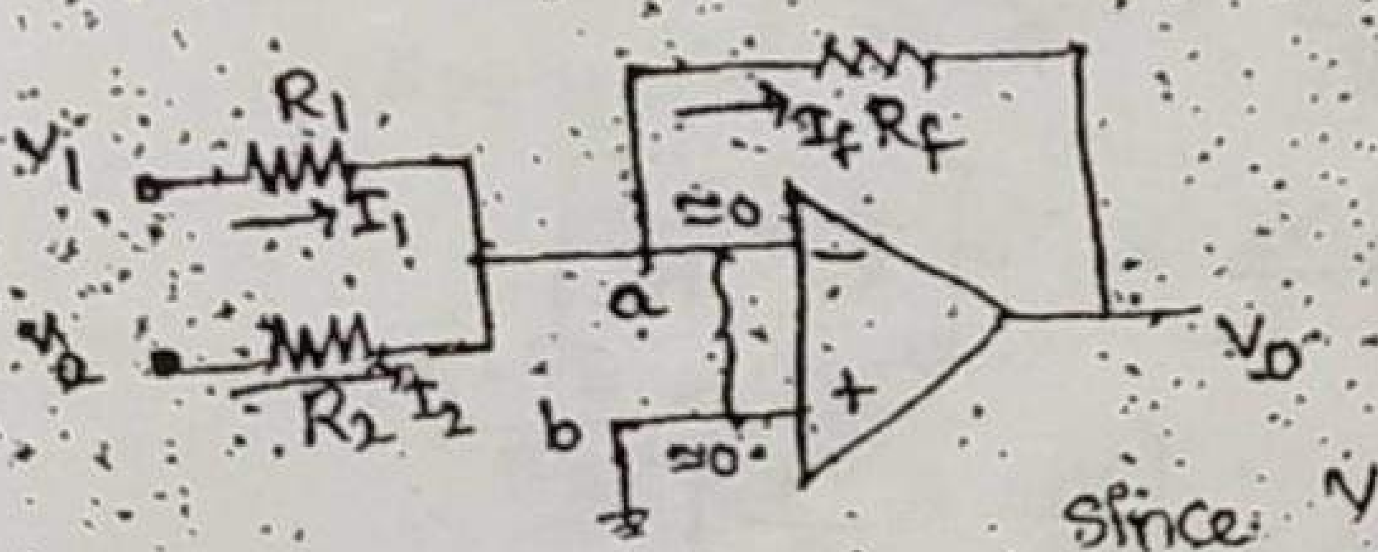
→ when $\frac{R_f}{R} = 0$ (i.e $R_f = 0$ & $R = \infty$).



As $V_0 = V_i$

* o/p voltage follows the i/p voltage
  - → voltage follower ckt
  - → voltage Buffer ckt

Summing Amplifier:-



since $V_d \simeq 0$

$$\boxed{V_b \simeq V_a}$$

But $V_b = 0$; $\boxed{V_a \simeq 0}$

Node 'a' – virtual ground.

Apply KCL at 'a'

$$I = I_f$$

$$\frac{0 - V_a}{R} = \frac{V_a - V_o}{R_f}$$

$$-\frac{R_f}{R} V_a = V_a - V_o$$

$$V_o = V_a\left(1 + \frac{R_f}{R}\right)$$

$$\boxed{V_o = \left(\frac{V_1 + V_2}{2}\right)\left(1 + \frac{R_f}{R}\right)}$$

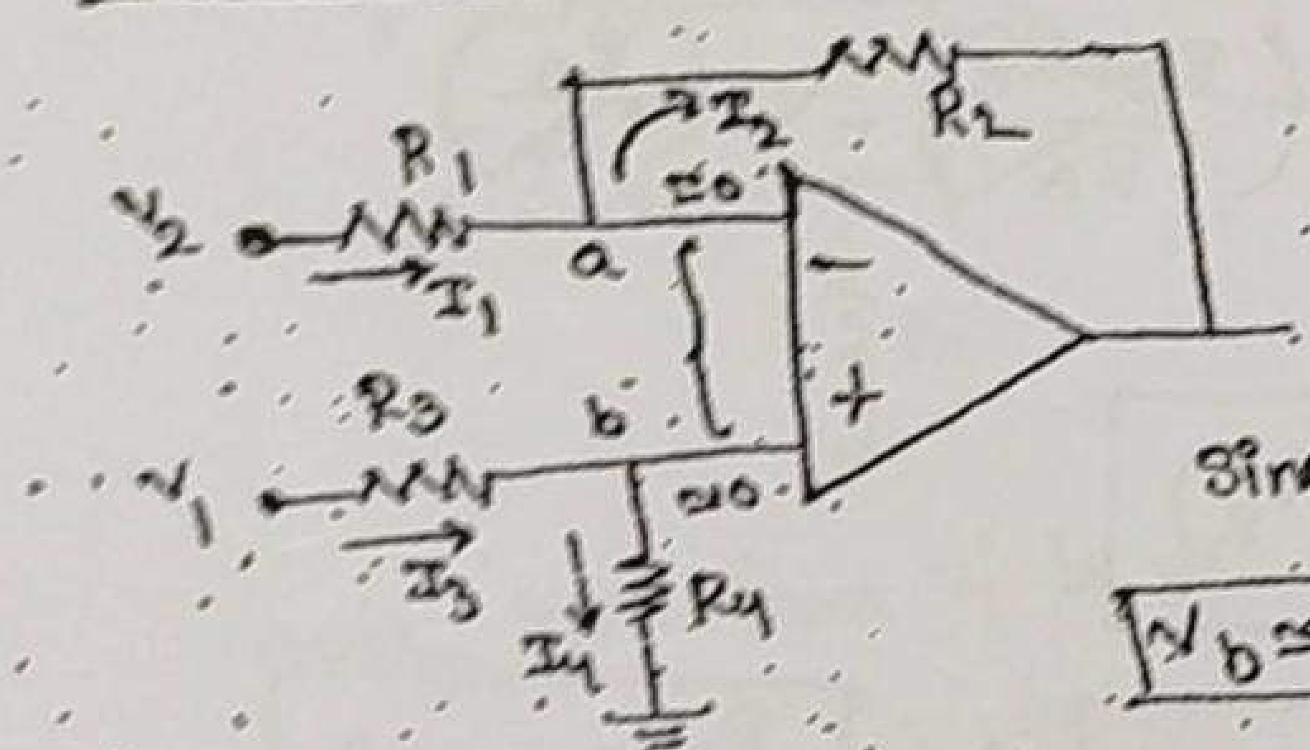
when $R_f = R$

$\boxed{V_o = (V_1 + V_2)}$ → summing amp.

when $\frac{R_f}{R} = 0$ (i.e $R_f = 0, R = \infty$)

$\boxed{V_o = \frac{V_1 + V_2}{2}}$ → Average amp.

Subtractor:-



Since $V_d \simeq 0$

$\boxed{V_b \simeq V_a}$

Apply KCL at b

$$I_3 = I_4$$

$$\frac{V_1 - V_b}{R_3} = \frac{V_b - 0}{R_4}$$

$$V_1 - V_b = R_3\left[\frac{V_b}{R_4}\right]$$

$$V_1 = V_b\left(1 + \frac{R_3}{R_4}\right)$$

$$\boxed{V_b = \frac{V_1}{\left(1 + \frac{R_3}{R_4}\right)}}$$

Scanned by TapScanner

Apply Kcl at 'a'

$$I_1 = I_2$$

$$\frac{V_2 - V_a}{R_1} = \frac{V_a - V_o}{R_2}$$

$$(V_2 - V_a) \times \frac{R_2}{R_1} = V_a - V_o$$

$$V_o = V_a\left(1 + \frac{R_2}{R_1}\right) - V_2\left(\frac{R_2}{R_1}\right)$$

$$\boxed{V_o = \frac{V_1}{\left(1 + \frac{R_3}{R_4}\right)}\left(1 + \frac{R_2}{R_1}\right) - V_2\left(\frac{R_2}{R_1}\right)}$$

when $R_1 = R_2$ & $R_3 = R_4$ $\Rightarrow$ $\boxed{V_o = V_1 - V_2}$ $\to$ subtractor.

NOTE:-

when $R_1 = R_3 = R_A$

$R_2 = R_4 = R_B$

$$V_o = \frac{V_1}{1 + \left(\frac{R_A}{R_B}\right)}\left(1 + \frac{R_B}{R_A}\right) - V_2\left(\frac{R_B}{R_A}\right)$$

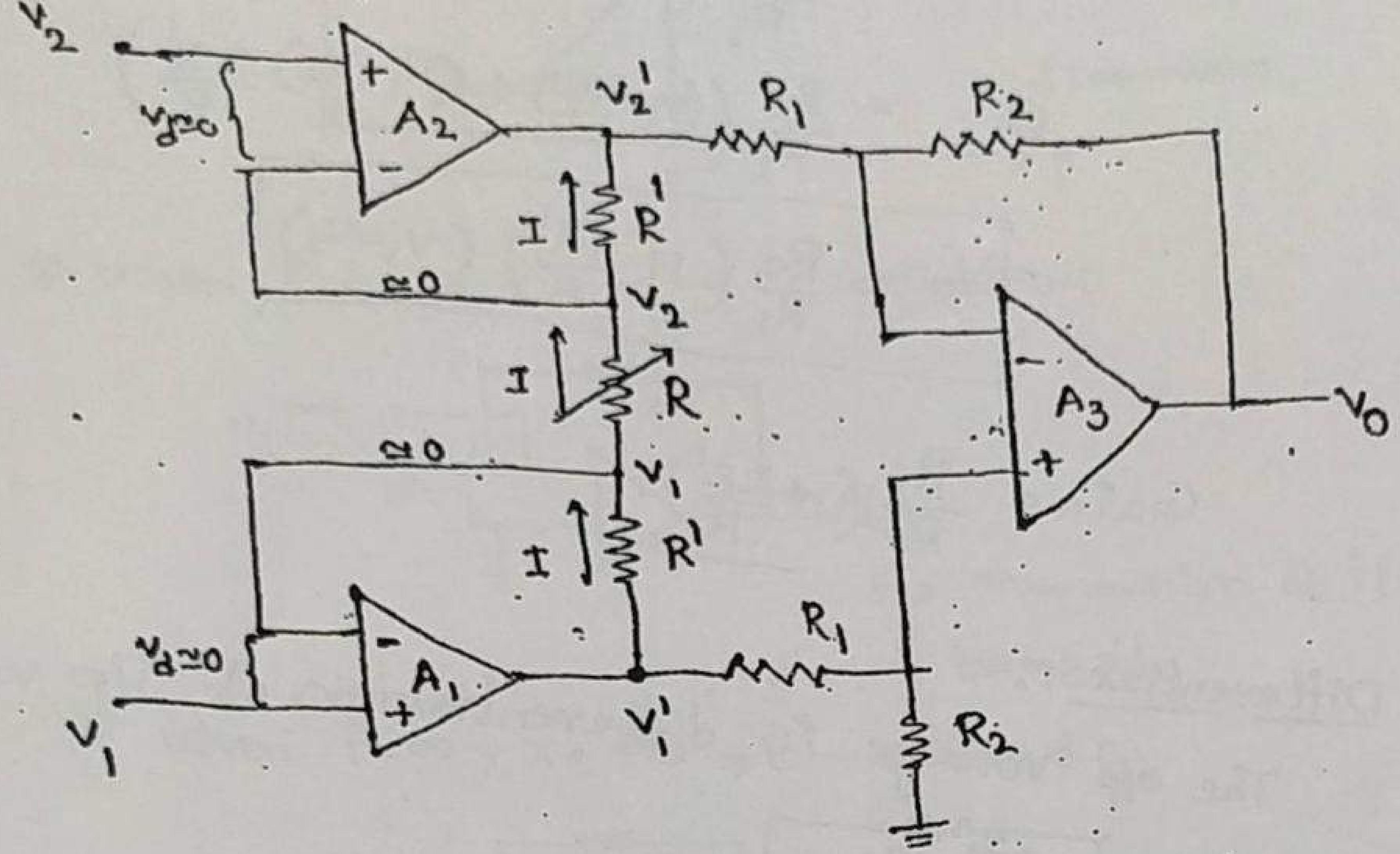
$$= \frac{V_1}{\left(\frac{\cancel{R_B + R_A}}{R_B}\right)}\left(\frac{\cancel{R_A + R_B}}{R_A}\right) - V_2\left(\frac{R_B}{R_A}\right)$$

$$\boxed{V_o = \frac{R_B}{R_A}(V_1 - V_2)}$$

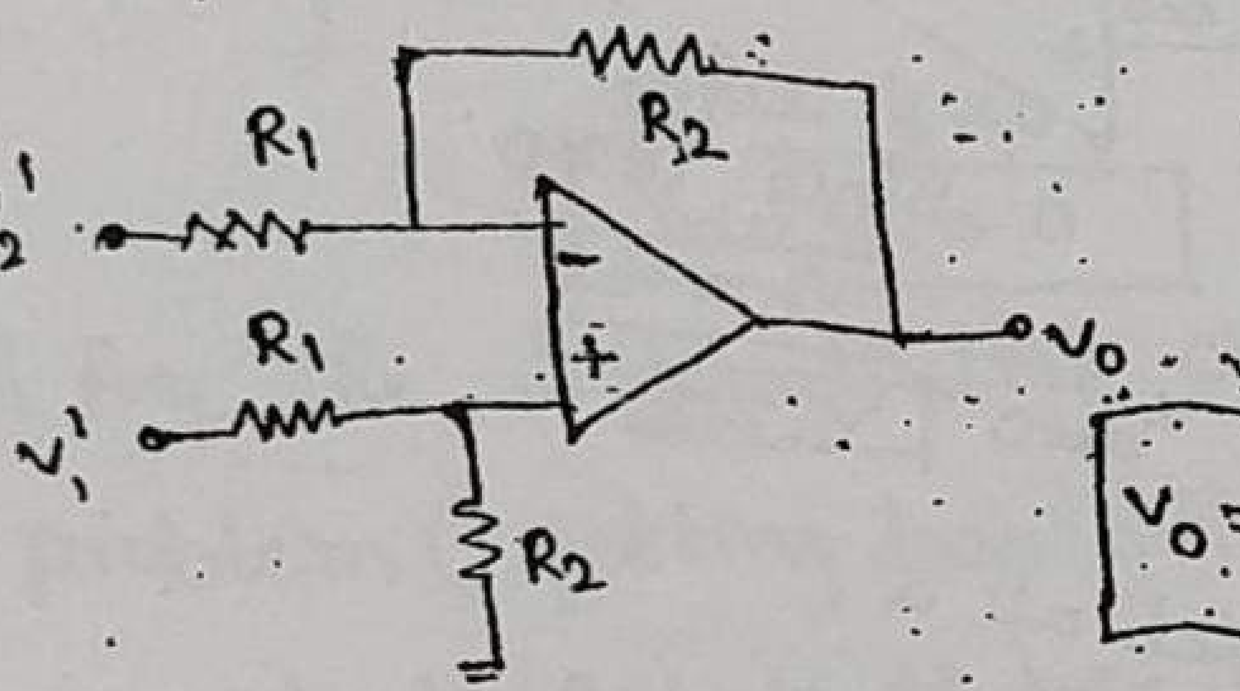
$$\boxed{V_o = \frac{R_2}{R_1}(V_1 - V_2)} \text{ (or) } \boxed{\frac{R_4}{R_3}(V_1 - V_2)}$$

Instrumentation Amp:-

High gain Amplifier



from the 3rd op-amp



$$\boxed{V_0 = \frac{R_2}{R_1}(V_1' - V_2')}$$

Apply KVL from V_1' to V_1

$$V_1' - IR' - V_1 = 0$$

$$\boxed{V_1' = IR' + V_1}$$

Apply KVL from V_2 to V_2'

$$V_2 - IR' - V_2' = 0$$

$$\boxed{V_2' = V_2 - IR'}$$

Substitute V_1' & V_2' in V_0

$$V_0 = \frac{R_2}{R_1}\left(IR' + V_1 - V_2 + IR'\right)$$

$$= \frac{R_2}{R_1}\left(V_1 - V_2 + 2IR'\right)$$

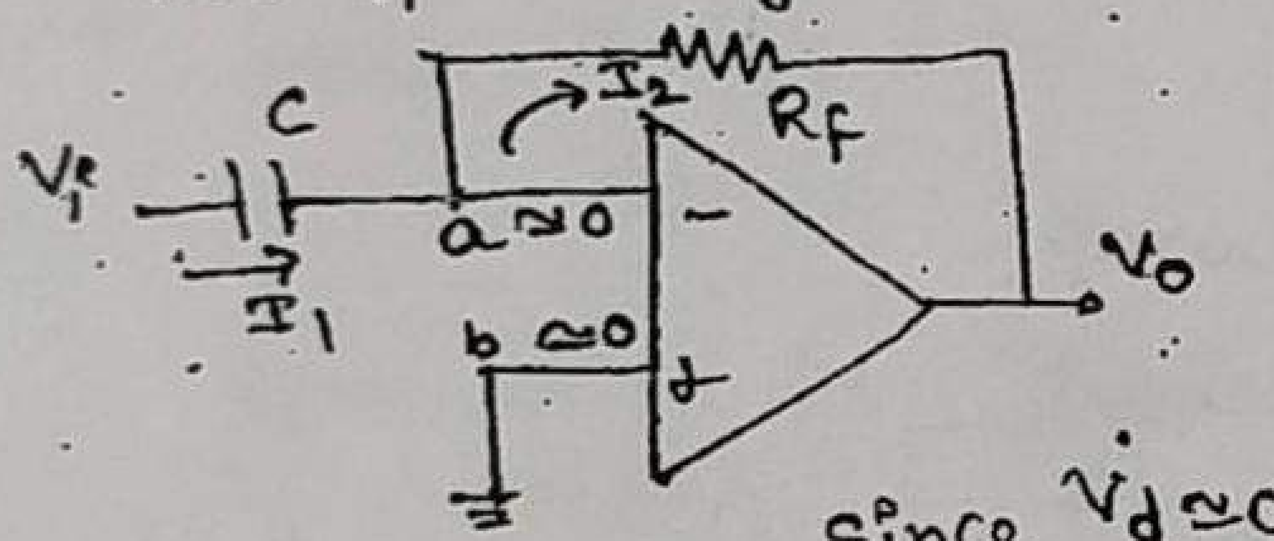
$$= \frac{R_2}{R_1}\left((V_1 - V_2) + (V_1 - V_2)\frac{2R'}{R}\right)$$

$$\boxed{V_0 = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_1 - V_2)}$$

$$\text{Gain} = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right).$$

Differentiator:-

The o/p voltage is differentiation of i/p voltage.



Since $V_d \simeq 0$

$\boxed{V_b \simeq V_a}$

But $V_b \simeq 0$ $\boxed{V_a \simeq 0}$

Apply KCL at 'a'

$$I_1 = I_2$$

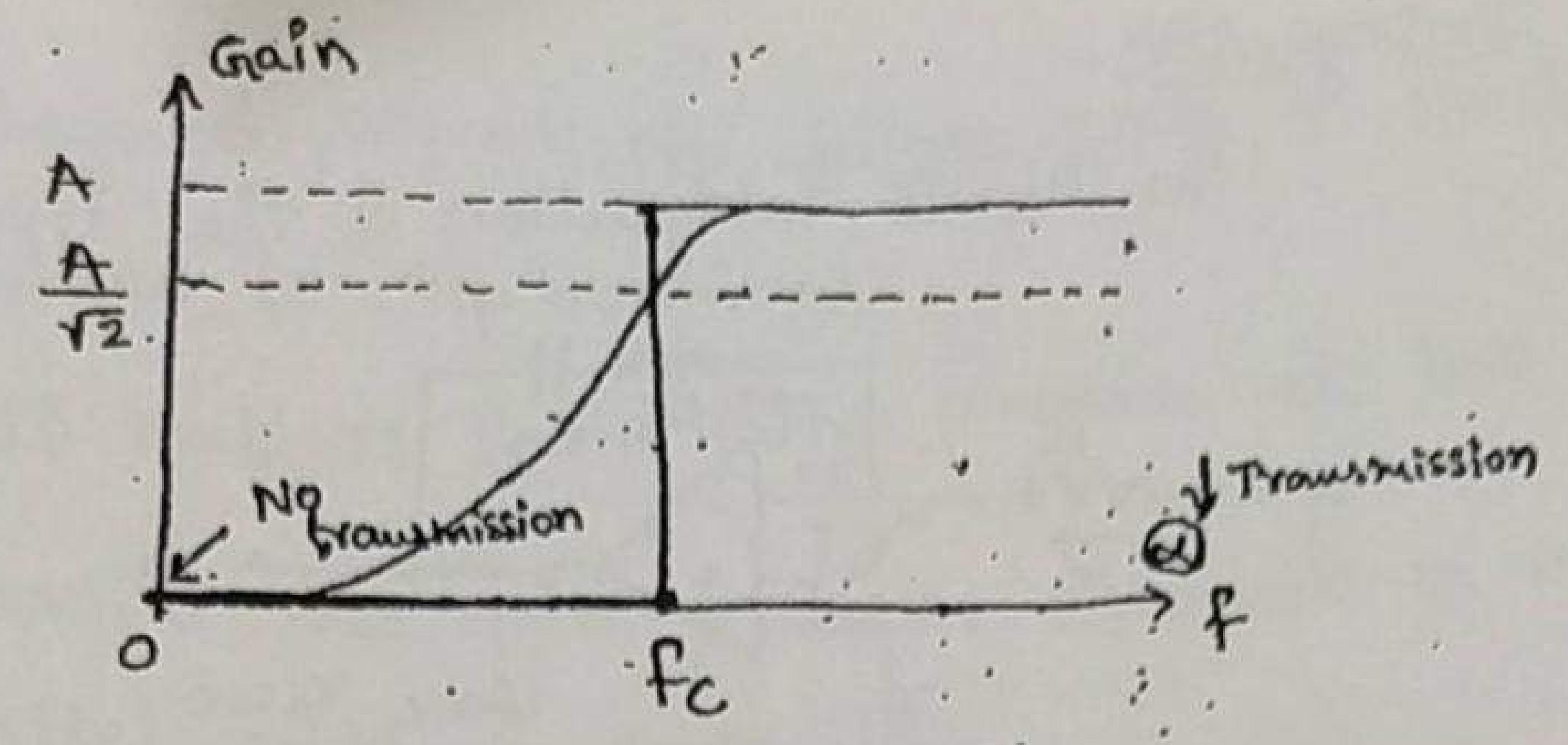
$$C\frac{d}{dt}(V_i - \cancel{V_a}^{0}) = \frac{(\cancel{V_a}^{0} - V_0)}{R_f}$$

$$C\frac{dV_i}{dt} = \frac{-V_0}{R_f}$$

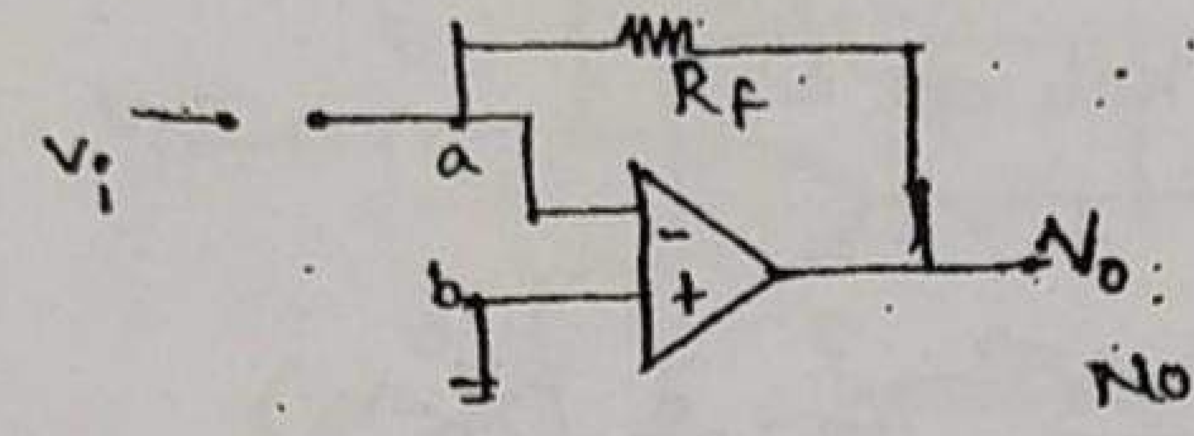
$$\boxed{V_0 = -R_f C \frac{dV_i}{dt}}$$

180° of phase shift b/w V_0 & V_i.

$\boxed{V_0 \propto \frac{dV_i}{dt}}$ → Differentiation is a high pass ckt i.e it allows all the high freq components of signal beyond its cut-off freq

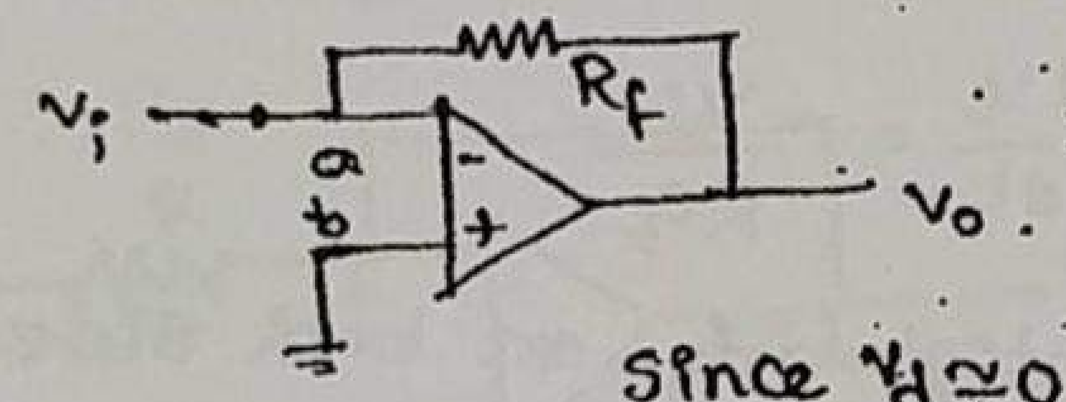


* when $f=0 \Rightarrow X_C=\infty \Rightarrow$ C-acts as O.C



No Transmission of i/p to o/p terminal.

* when $f=\infty$, $X_C=0 \Rightarrow$ C - acts as S.C

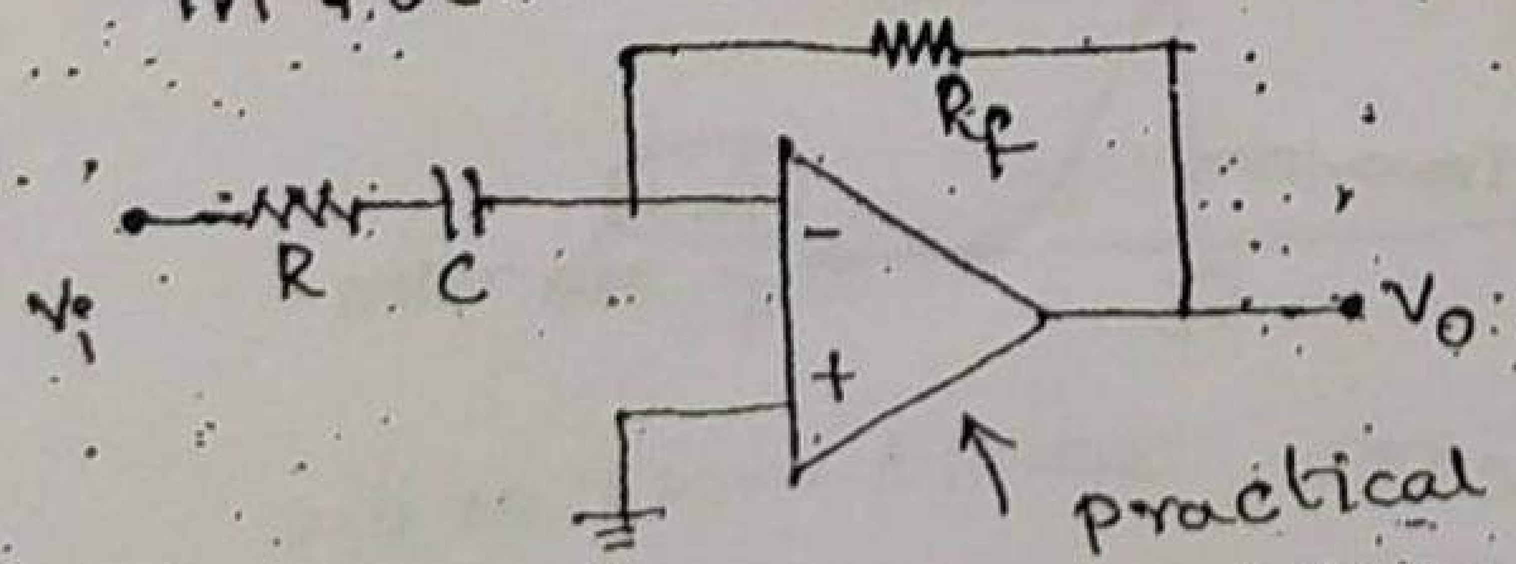


Since $V_d \simeq 0$

$$\boxed{V_b \simeq V_a \simeq 0}$$

* At high freq the differentiators ckt sufferes from Noise problem (getting two different potentials on a short ckt line but that is impossible). To overcom this noise problem.

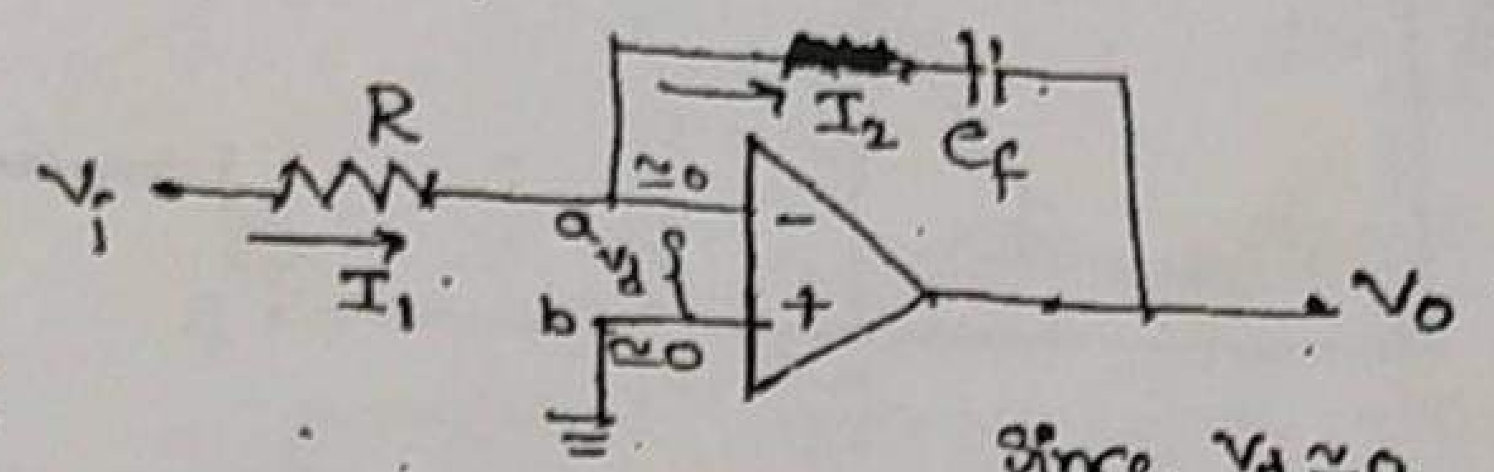
* To avoid that noise problem, A Resistor is connecte in series with capacitor.



practical Differentiator ckt.

Integrator:-

The o/p is integration of the i/p.



Since $V_d \simeq 0$

$$\boxed{V_b \simeq V_a \simeq 0}$$

Apply KCL at 'a'.

$$I_1 = I_2$$

$$\frac{V_i - \cancel{V_a}^{0}}{R} = C_f \cdot \frac{d}{dt}(\cancel{V_a}^{0} - V_o)$$

$$\frac{V_i}{R} = -C_f \frac{dV_o}{dt}$$

$$\frac{dV_o}{dt} = -\frac{V_i}{RC_f}$$

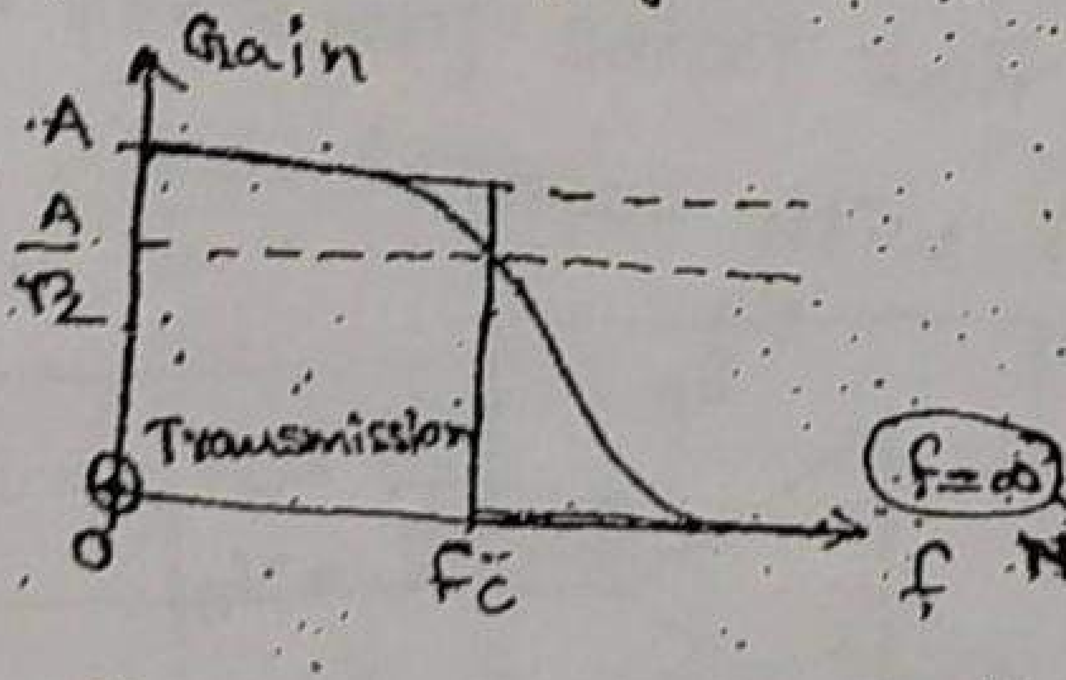
Integrating on both sides

$$\boxed{V_o = -\frac{1}{RC_f}\int V_i \, dt}$$

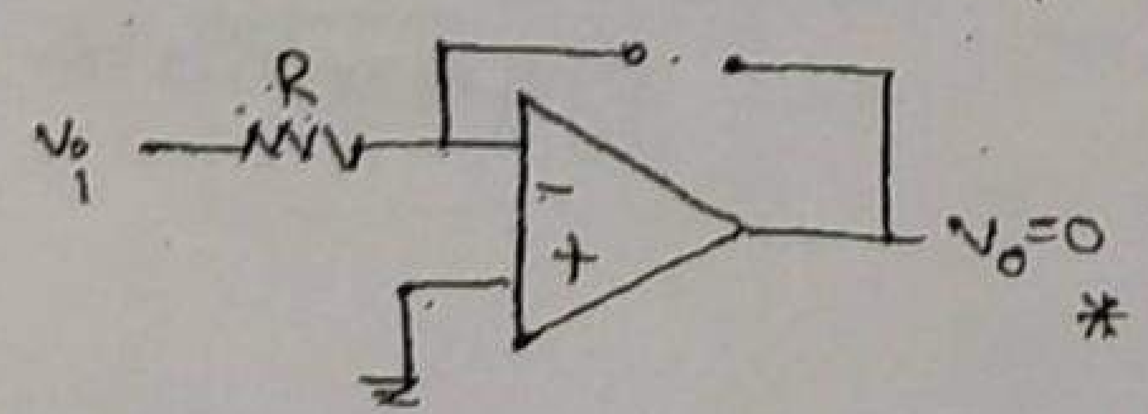
180° of phase b/w V_o & V_i.

$$\boxed{V_o \propto \int V_i \, dt}$$

- Integrator is a low pass ckt ie it allows all the freq components of signal upto its cutoff freq.



* when $f=0$, $X_C=\infty$, capacitor → act as o.c

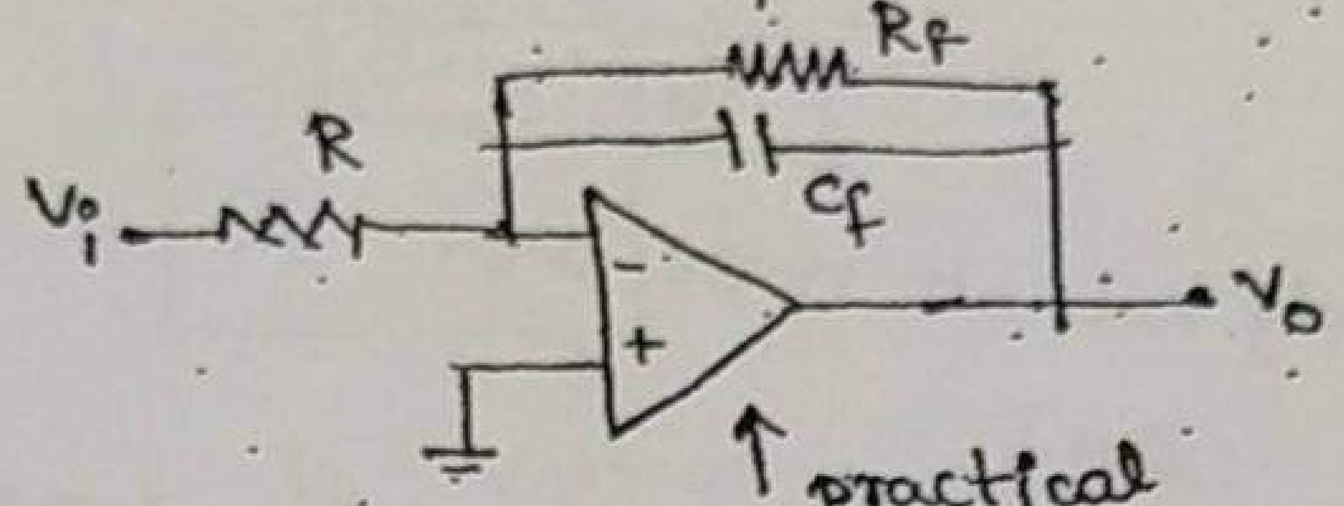


* No i/p signal transmitted to o/p terminal.

* The integrator signal o/p voltage zero & No i/p signal transmitted to o/p terminal.

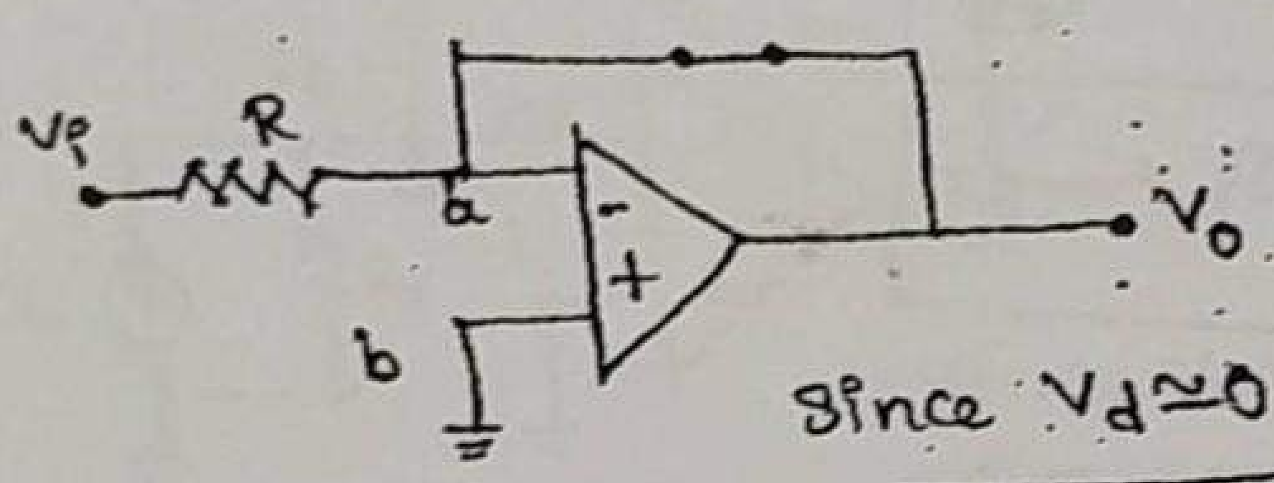
It suffers from gain problem at low frequencies.

* To avoid the gain problem connect a resistor in parallel with a capacitor.



practical integrator ckt.

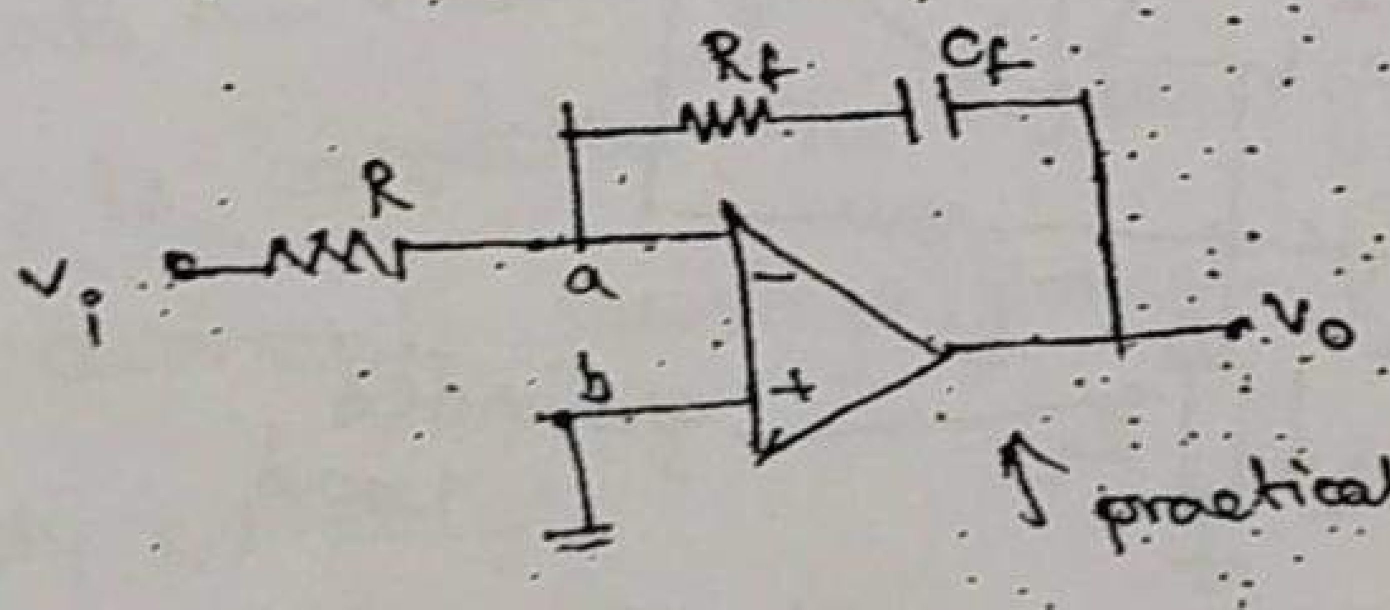
* when $f=\infty$, $X_c=0$ c→acts as S.C



since $V_d \simeq 0$

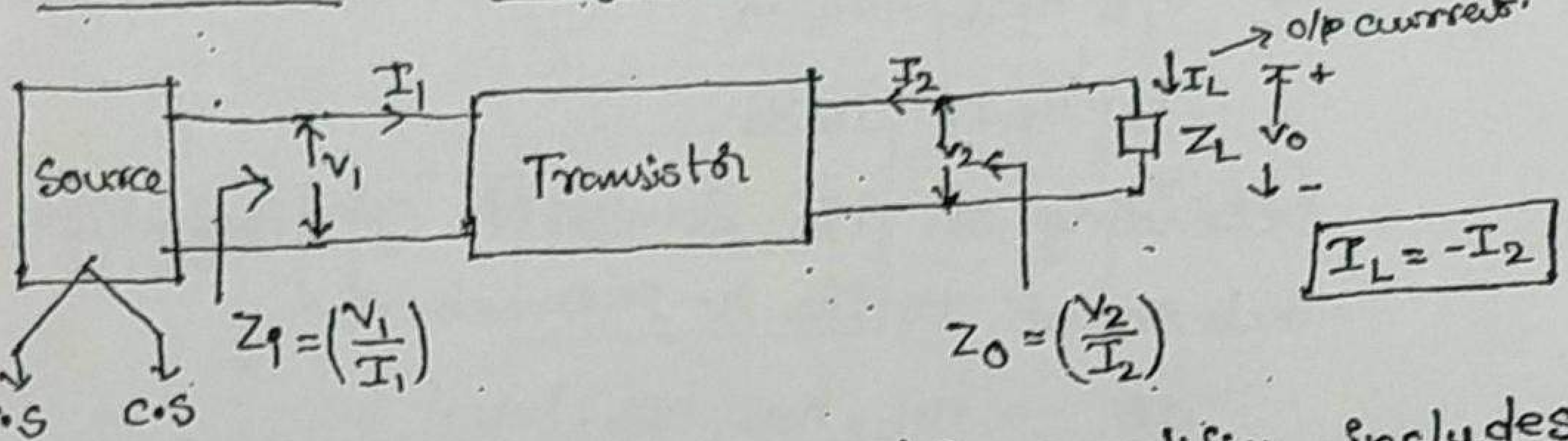
$\boxed{V_b \simeq V_a \simeq 0}$

$V_o = V_a = 0$ →(No. txion).



practical integrator ckt.

Transistor Amp. Analysis using h-parameters :-



* The Analysis of the transistor amplifier includes the calculation of the following

① current gain , $A_I = \left(\frac{I_L}{I_1}\right)$

② Input impedance, $Z_i = \left(\frac{V_1}{I_1}\right)$

③ Voltage gain , $A_V = \left(\frac{V_0}{V_1}\right)$

④ Output impedance, $Z_0 = \left(\frac{V_2}{I_2}\right)$

⑤ voltage amplification (or) overall voltage gain $\Rightarrow$ $\boxed{A_{VS} = \left(\frac{V_0}{V_S}\right)}$

⑥ current Amplification (or) overall current gain $\Rightarrow$ $\boxed{A_{IS} = \left(\frac{I_L}{I_S}\right)}$

$$\left\{\begin{array}{l} V_1 = h_i I_1 + h_r V_2 \\ I_2 = h_f I_1 + h_o V_2 \end{array}\right\} \text{ use these eqn's.}$$

1. current gain :- (A_I)

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

$I_2 = h_f I_1 + h_o V_2$ But $V_2 = V_0 = I_L Z_L$

$= -I_2 Z_L$

$$I_2 = h_f I_1 + h_o(-I_2 Z_L)$$

$$I_2(1+h_o Z_L) = h_f I_1$$

$$\left(\frac{I_2}{I_1}\right) = \frac{h_f}{(1+h_o Z_L)}$$

$$\boxed{A_I = \frac{-I_2}{I_1} = \frac{-h_f}{(1+h_o Z_L)}}$$

② Input impedance:-

$$Z_i = \frac{V_1}{I_1}$$

$$V_1 = h_i I_1 + h_r V_2$$

$$V_1 = h_i I_1 + h_r(-I_2 Z_L)$$

$$= I_1\left(h_i + h_r\left(\frac{-I_2}{I_1}\right) Z_L\right)$$

$$\therefore \boxed{Z_i = \frac{V_1}{I_1} = h_i + h_r A_I Z_L}$$

(or) $Z_i = h_i + h_r\left(\frac{-h_f}{1+h_o Z_L}\right) Z_L$

$$= h_i - \frac{h_r h_f}{1+h_o Z_L} \times Z_L$$

$$= h_i - \frac{h_r h_f}{\left(\frac{1+h_o Z_L}{Z_L}\right)}$$

$$\therefore \boxed{Z_i = h_i - \frac{h_r h_f}{\left(\frac{1}{Z_L} + h_o\right)}}$$

③ Voltage gain:-

$$A_V = \frac{V_o}{V_1} = \frac{V_2}{V_1}$$

$$A_V = \left(\frac{-I_2 Z_L}{V_1}\right)$$

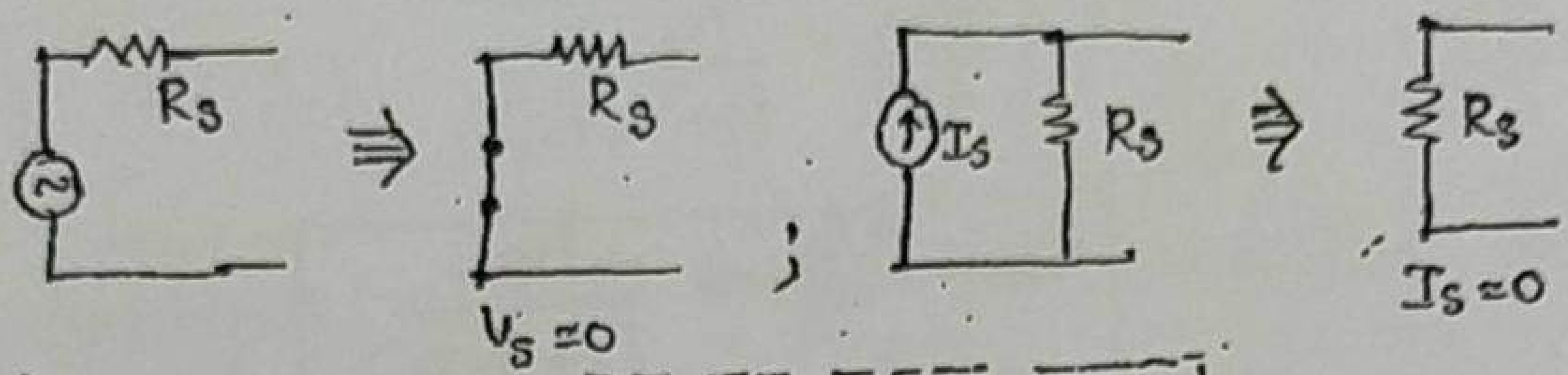
$$\frac{V_1}{I_1} = Z_i \Rightarrow V_1 = Z_i I_1$$

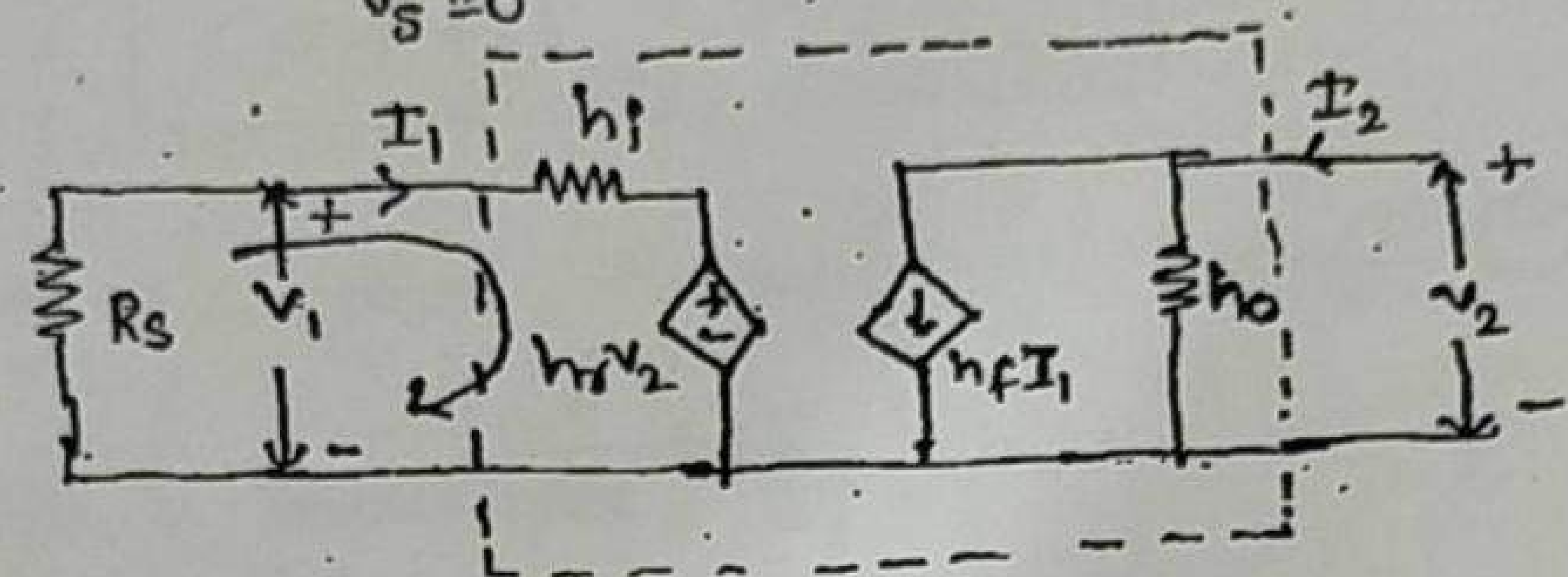
$$A_V = \frac{-I_2 Z_L}{Z_i \cdot I_1} = \left(-\frac{I_2}{I_1}\right) \cdot \frac{Z_L}{Z_i}$$

$$\boxed{A_V = \frac{A_I Z_L}{Z_i}}$$

(4) output impedance :-

$$Z_o = \left(\frac{V_2}{I_2}\right) \Bigg|\ \begin{array}{l}\text{Load} \rightarrow \text{o.c \&} \\ \text{All the sources set equal to zero.}\end{array}$$





$$I_2 = h_f I_1 + h_o V_2$$
$$= V_2\left[h_o + h_f \frac{I_1}{V_2}\right]$$

$$\frac{I_2}{V_2} = \frac{1}{Z_o} = Y_o = h_o + h_f\left(\frac{I_1}{V_2}\right)$$

To calculate Z_o, first calculate $\left(\frac{I_1}{V_2}\right)$

Apply KVL to i/p loop.

$$0 - I_1(R_s + h_i) - h_r V_2 = 0$$
$$I_1(R_s + h_i) = -h_r V_2$$
$$\frac{I_1}{V_2} = \left(\frac{-h_r}{R_s + h_i}\right)$$

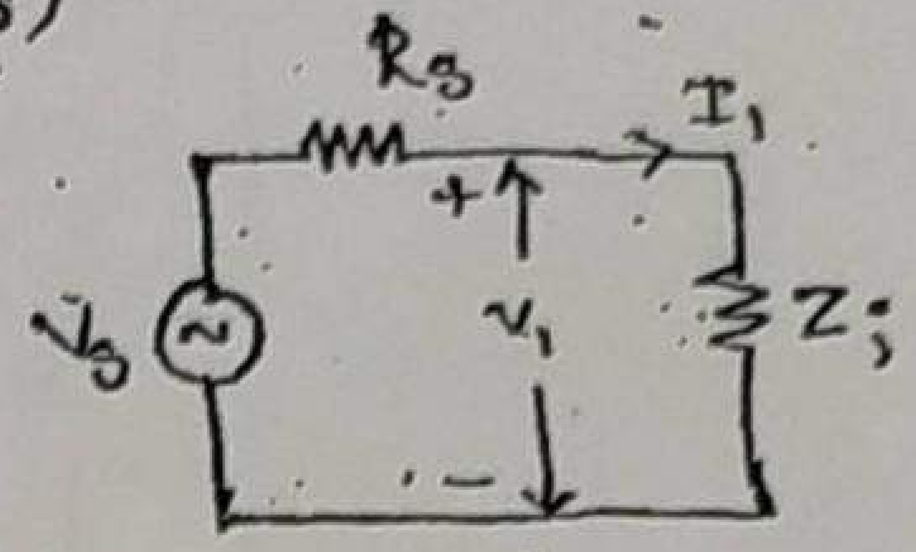
$$Y_o = h_o + h_f\left(\frac{-h_r}{R_s + h_i}\right) = h_o - \frac{h_r h_f}{R_s + h_i}$$

$$\boxed{Y_o = h_o - \frac{h_r h_f}{R_s + h_i}} \qquad Z_o = \frac{1}{Y_o}$$

Voltage amplification :-

$$A_{VS} = \frac{V_o}{V_S} = \left(\frac{V_o}{V_1}\right)\left(\frac{V_1}{V_S}\right)$$

$$\Rightarrow A_{VS} = A_V\left(\frac{V_1}{V_S}\right)$$



$$V_1 = V_S\left(\frac{Z_i}{R_S+Z_i}\right)$$

$$\left(\frac{V_1}{V_S}\right) = \frac{Z_i}{R_S+Z_i}$$

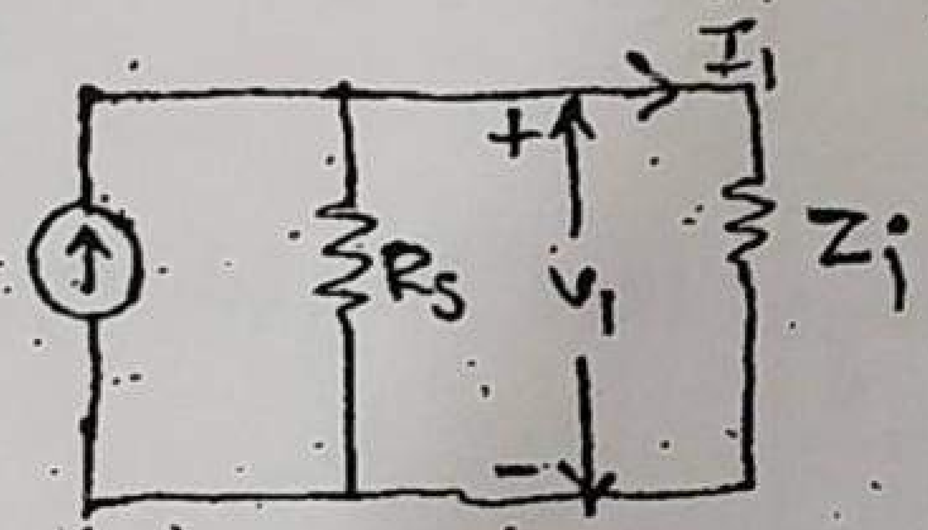
$$A_{VS} = A_V\underbrace{\left(\frac{Z_i}{R_S+Z_i}\right)}_{<1} \qquad \boxed{A_{VS} < A_V}$$

for an ideal voltage source, $R_S = 0$.

$$\boxed{A_{VS} = A_V}$$

Current amplification :-

$$A_{IS} = \left(\frac{I_L}{I_S}\right) = \left(\frac{I_L}{I_1}\right)\cdot\left(\frac{I_1}{I_S}\right) \Rightarrow \boxed{A_{IS} = A_I\left(\frac{I_1}{I_S}\right)}$$



$$\Rightarrow I_1 = I_S\left(\frac{R_S}{R_S+Z_i}\right)$$

$$\therefore \boxed{A_{IS} = A_I\left(\frac{R_S}{R_S+Z_i}\right)}$$

$$\Rightarrow A_{IS} < A_I$$

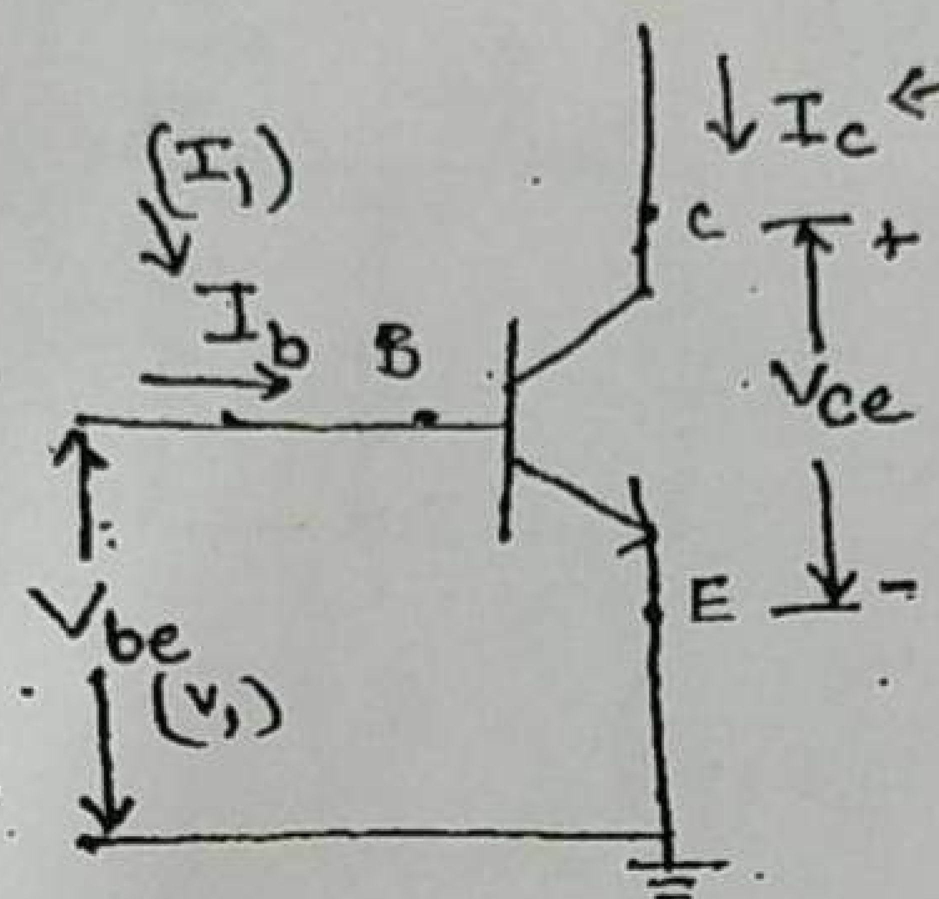
for an ideal current source $R_S = \infty$.

$$A_{IS} = A_I\left(\frac{1}{1+\cancel{\frac{Z_i}{R_S}}\,0}\right)$$

$$\boxed{A_{IS} = A_I}$$

* Simplified (or) Approximate model:-

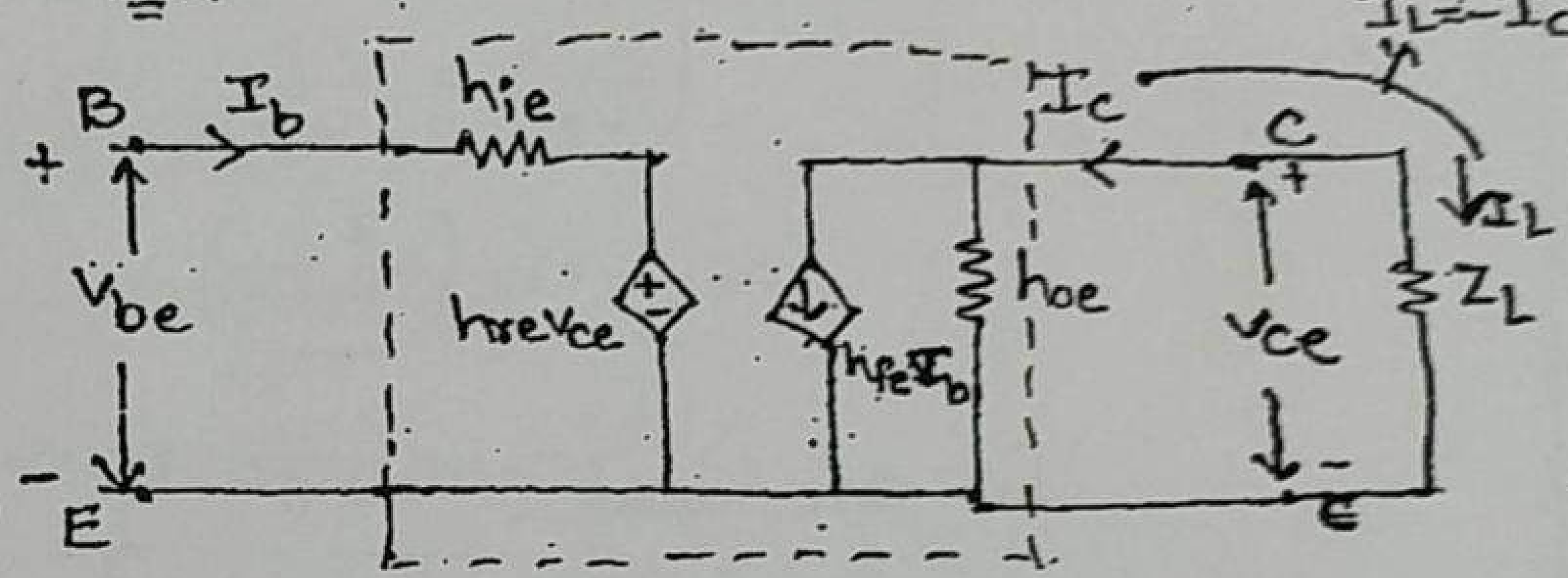
This model based on CE → we must use h-parameters of CE only. i.e (h_{ie}, h_{re}, h_{fe}, h_{oe}).



V_{be} → AC signal
V_{BE} → DC signal *

$$V_{be} = h_{ie} I_b + \cancel{h_{re} V_{ce}}$$

$$I_c = h_{fe} I_b + \cancel{h_{oe} V_{ce}}$$



In simplified model we neglect $\left\{ \begin{array}{l} h_{re} V_{ce} \\ h_{oe} V_{ce} \end{array} \right\}$

<u>Reason for neglecting $h_{oe} V_{ce}$</u>:-

$$h_{oe} = 25\mu℧$$

$$\frac{1}{h_{oe}} = \frac{1}{25\mu} = 40k\Omega$$

In generally Z_L is always less than (or) equal to $5k\Omega$

$$Z_L \parallel \frac{1}{h_{oe}} \simeq Z_L$$

As $\frac{1}{h_{oe}}$ is very high - the current passing through it is very low ($\simeq 0$).

$h_{oe} V_{ce}$ → neglected (or)
→ O.C.

$$\boxed{I_c = h_{fe} I_b}$$

Reason for neglecting $h_{re}V_{ce}$:-

$$h_{re}V_{ce} = h_{re}(I_L Z_L)$$
$$= h_{re}(-I_c)Z_L$$
$$= h_{re}(-h_{fe}I_b)Z_L$$
$$= -h_{re}h_{fe}I_bZ_L$$
$$= -2.5\times10^{-4}\times 50\, I_bZ_L$$

$$\boxed{h_{re}V_{ce} = -12.5\times10^{-3} I_b Z_L}$$

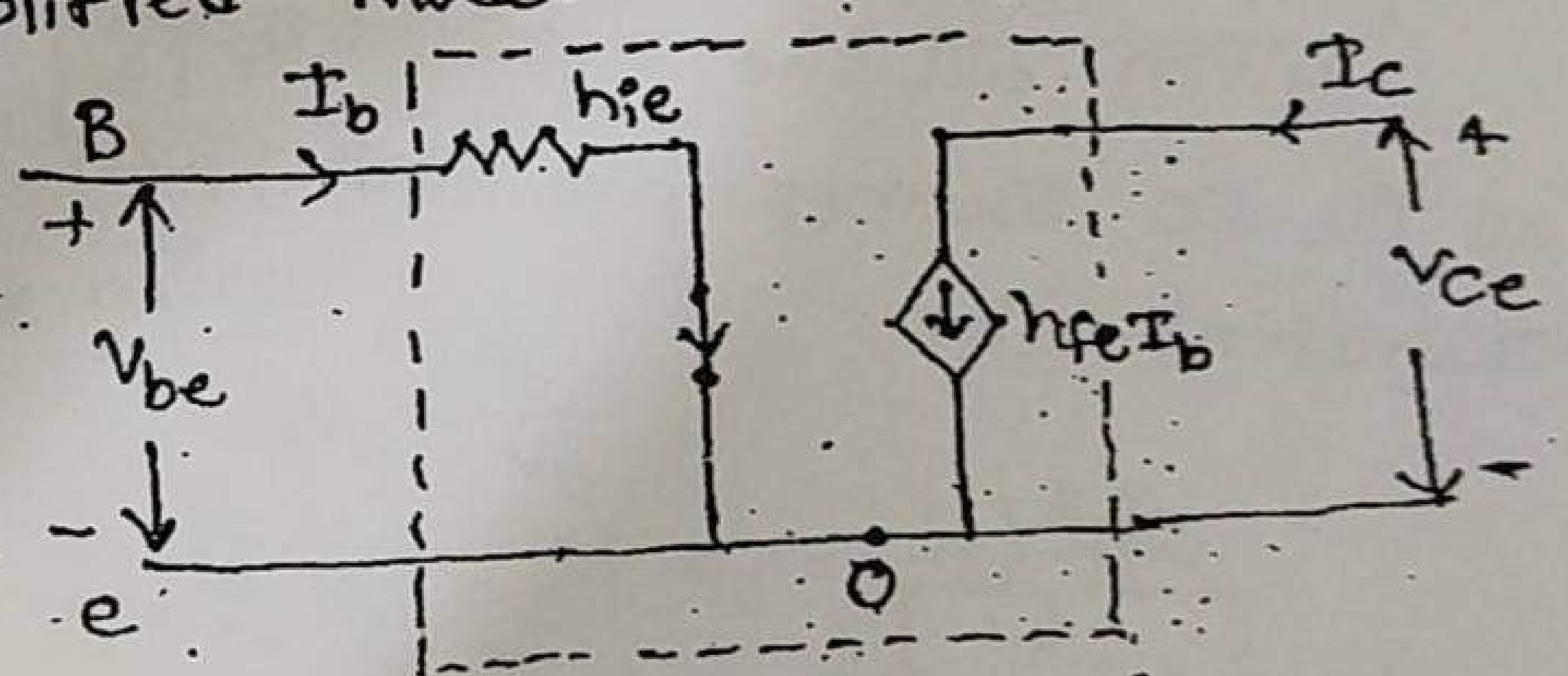
$$V_{be} = h_{ie}I_b + \underbrace{h_{re}V_{ce}}_{\text{(neglected)}}$$

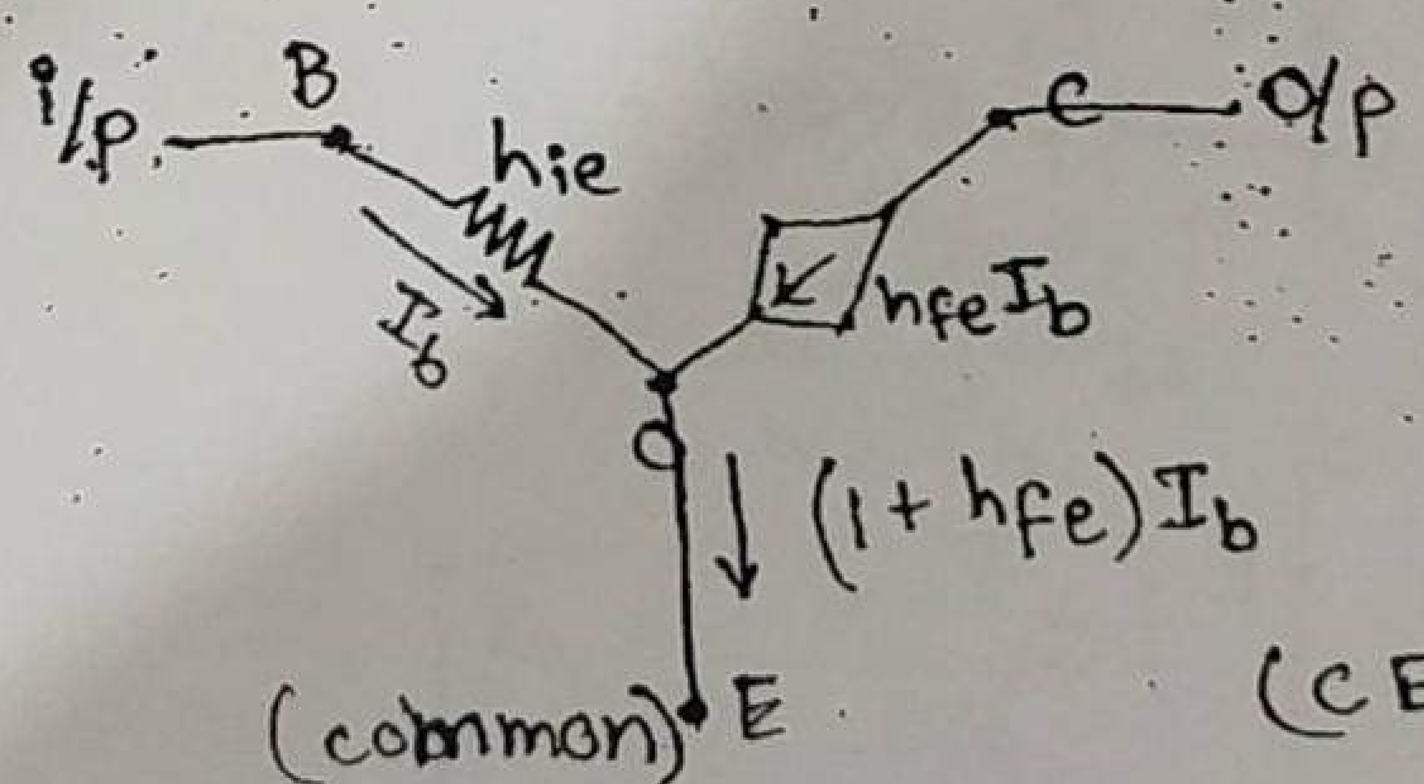
$$\underbrace{V_{be}}_{mV} = \underbrace{h_{ie}I_b}_{K\Omega\ \mu A \to mV} \underbrace{-12.5\times10^{-3}\underbrace{I_b Z_L}_{\mu A\ K\Omega \to mV}}_{\mu V}$$

→ $h_{re}V_{ce}$ - neglected (or) (s.c).

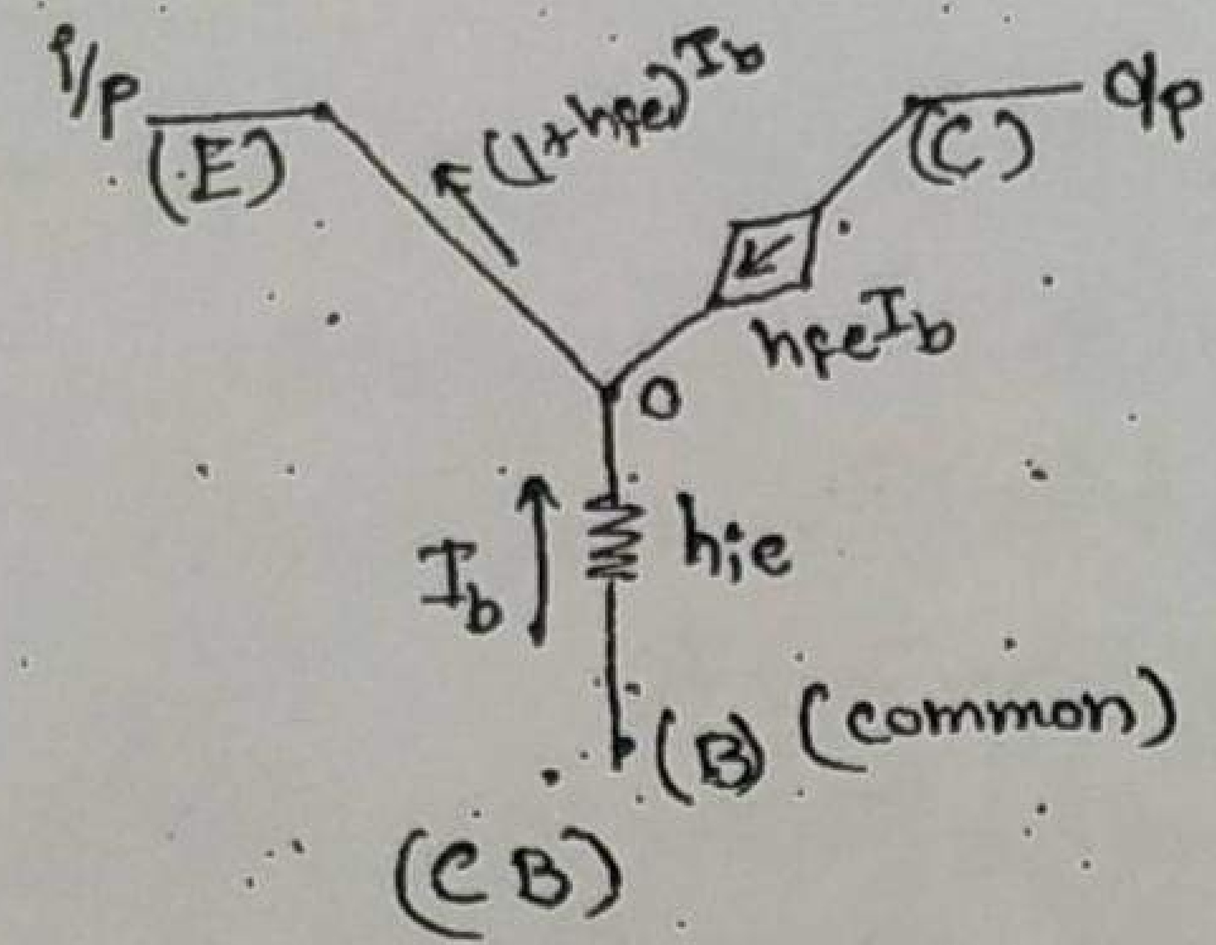
$$\boxed{V_{be} = h_{ie}I_b} \quad \& \quad \boxed{I_c = h_{fe}I_b}$$

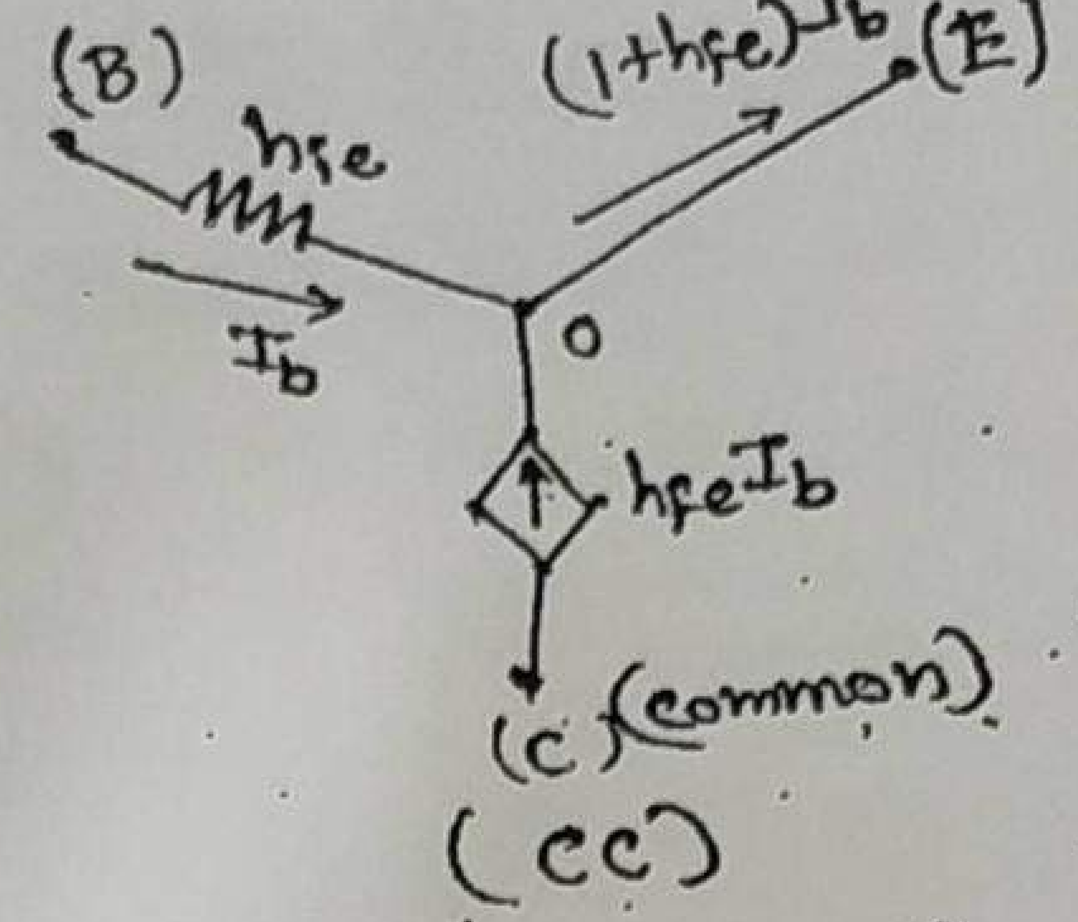
The simplified model of the transistor is





(CE)

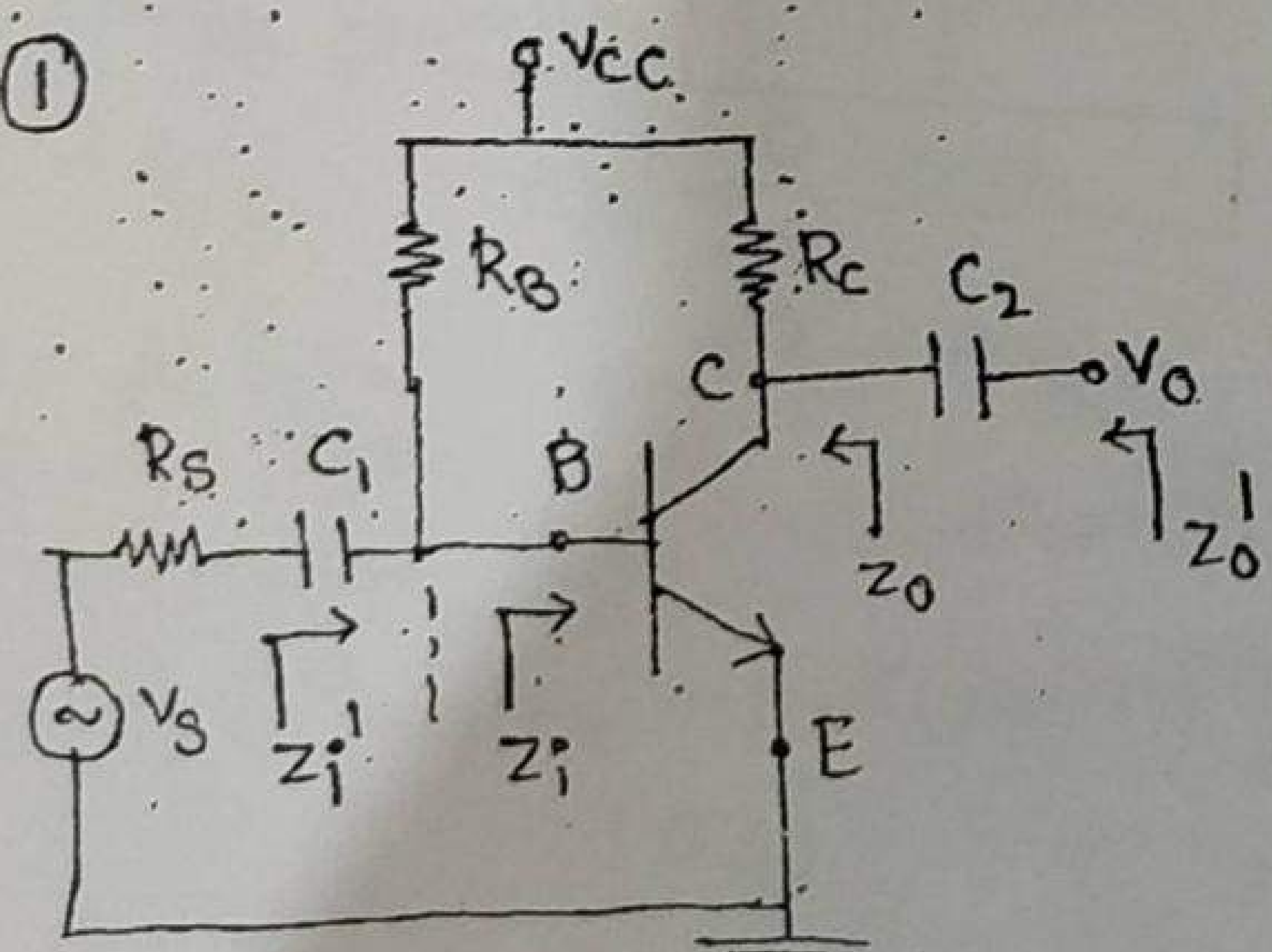


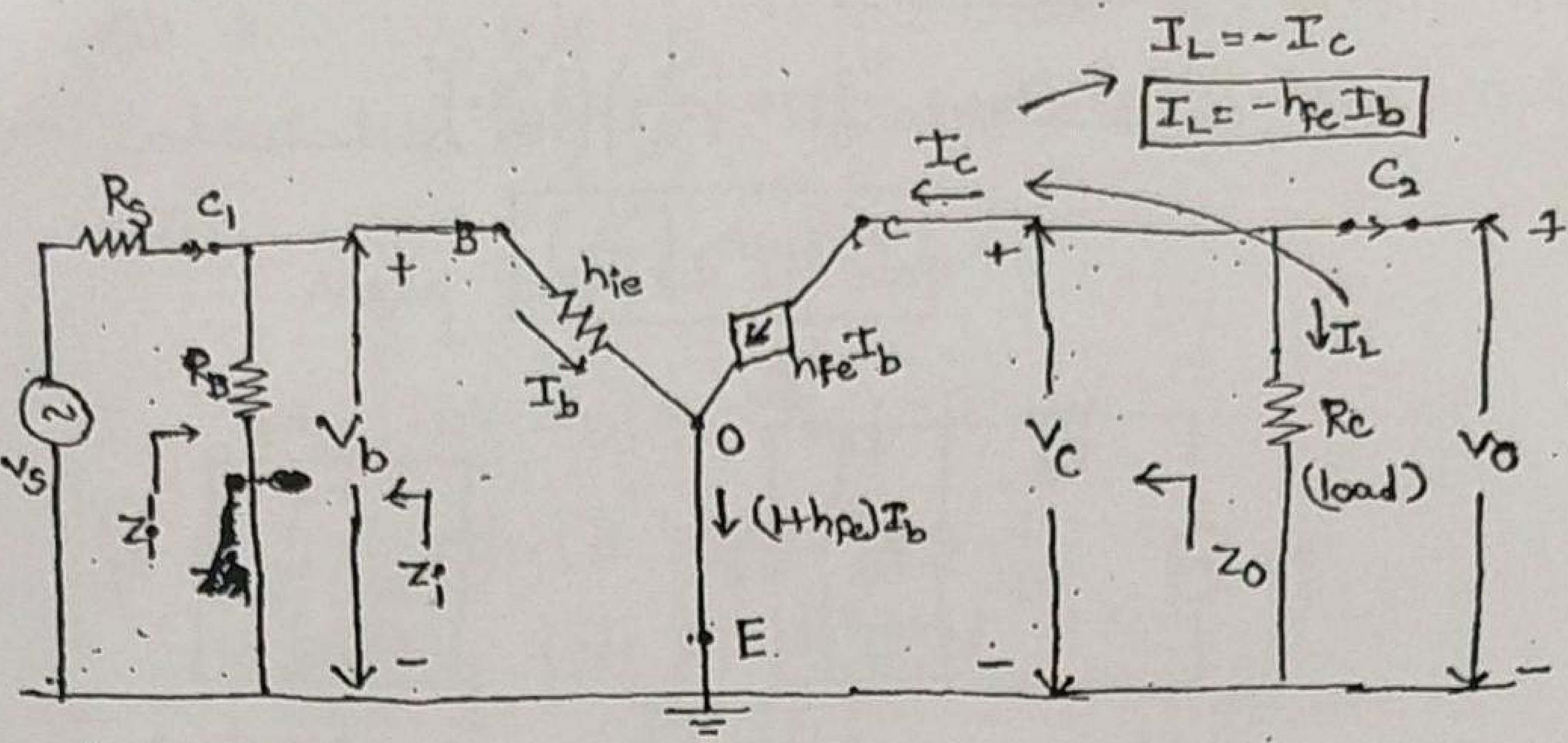


<u>Procedure to draw the AC equivalent ckt of a given Amplifier ckt:-</u>

1. Replace the transistor by its equivalent simplified model
2. Connect the ckt components at common, i/p & o/p terminal.
   (i) connect the resistors directly.
   (ii) when freq of signal & cap. values are given, calculate the reactance of each capacitor.
   if $X_C \to$ veryhigh $\Rightarrow$ All the 'C' are replaced by o.c.
   $X_C \to$ very low $\Rightarrow$ 'C' are replaced by s.c.
   (iii) when freq of signal (or) capacitance value not given all the capacitors are replaced by s.c.
3. All the DC sources are set equal to zero in the AC equivalent ckt.

(1)





1. Current gain :-

$$A_I = \frac{I_L}{I_b} = \frac{-h_{fe} I_b}{I_b} = -h_{fe}.$$

2. Input impedance :-

$$\boxed{Z_i = \frac{V_b}{I_b}}$$

$$\boxed{V_b \doteq h_{ie} I_b} \rightarrow ①$$

$$Z_i = \frac{h_{ie} I_b}{I_b} = h_{ie}.$$

$$\therefore \boxed{Z_i = h_{ie}}$$

$$\boxed{Z_i' = Z_i \parallel R_B}$$

3. Voltage gain :-

$$A_V = \frac{V_o}{V_b}$$

$$V_o = I_L R_C = -I_2 R_C = -h_{fe} I_b R_C$$

eq ①
$$V_b = h_{ie} I_b$$

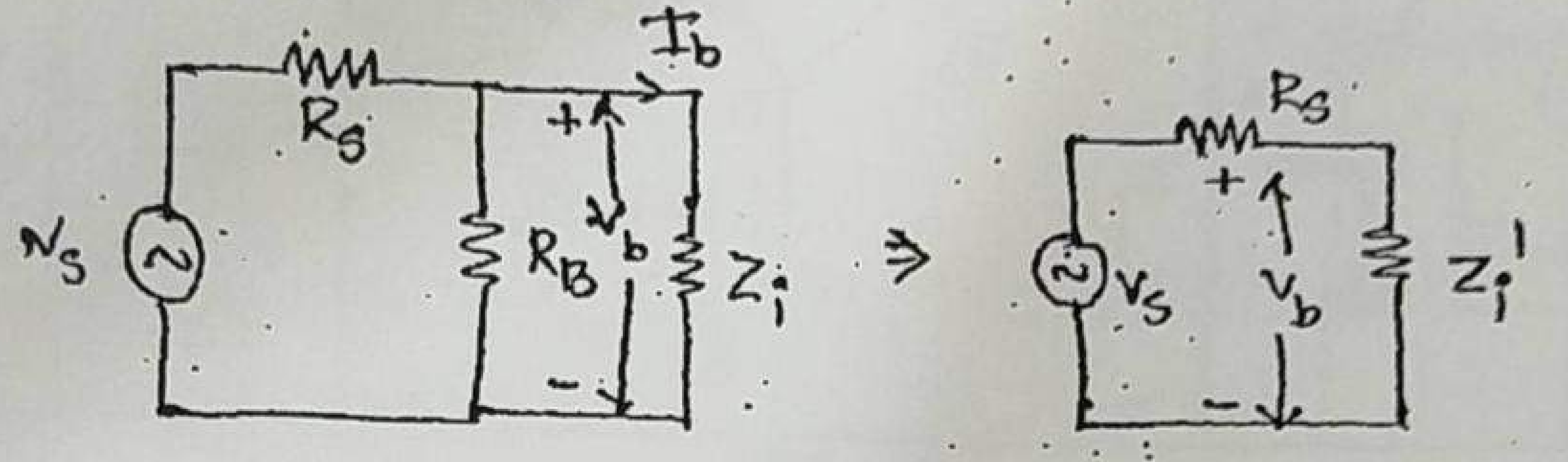
$$A_V = \frac{-h_{fe} I_b R_c}{h_{ie} I_b}$$

$$\boxed{A_V = -\frac{h_{fe} R_c}{h_{ie}}}$$

Voltage amplification:-

$$A_{vs} = \frac{V_o}{V_s} = \left(\frac{V_o}{V_b}\right)\left(\frac{V_b}{V_s}\right)$$

$$\boxed{A_{vs} = A_v\left(\frac{V_b}{V_s}\right)}$$



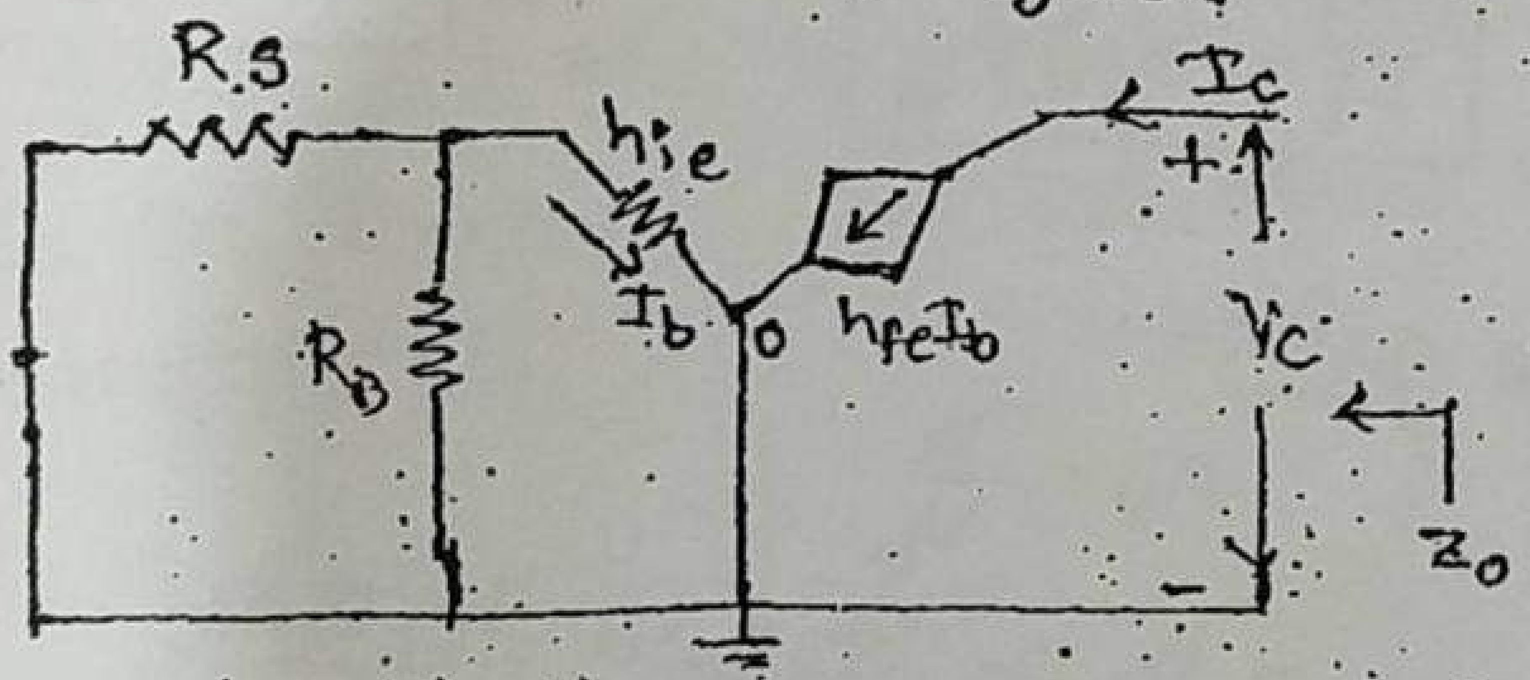
$$V_b = V_s\left(\frac{Z_i'}{Z_i'+R_s}\right)$$

$$A_{vs} = A_v \frac{\cancel{V_s}\left(\frac{Z_i'}{Z_i'+R_s}\right)}{\cancel{V_s}}$$

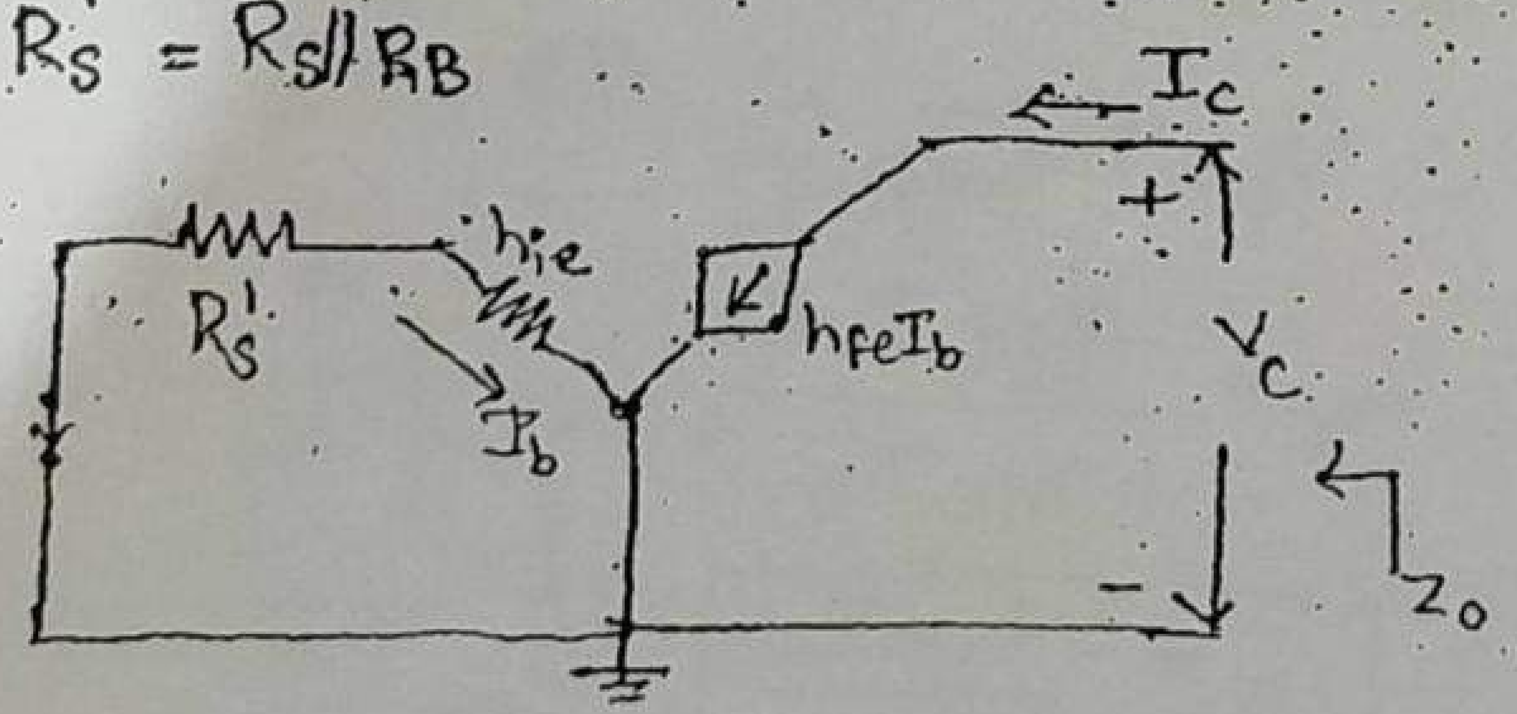
$$\boxed{A_{vs} = A_v\left(\frac{Z_i'}{Z_i'+R_s}\right)}$$

output impedance:-

$$Z_o = \left.\frac{V_c}{I_c}\right| \begin{array}{l} R_C \to O.C \\ V_s = 0V \end{array}$$



$R_s' = R_s \| R_B$



As it is not possible to calculate V_c, go for the calculation of I_c. To calculate I_c, first calculat I_b.

Apply KVL to i/p loop

$$0 - I_b(R_s' + h_{ie}) = 0$$

$$I_b(R_s' + h_{ie}) = 0$$

To satisfy this condition,

$$\boxed{I_b = 0}$$

$$I_c = h_{fe} I_b = 0.$$

$$\Rightarrow \boxed{Z_0 = \frac{V_c}{I_c} = \infty}$$

$$\Rightarrow Z_0' = Z_0 // R_c$$

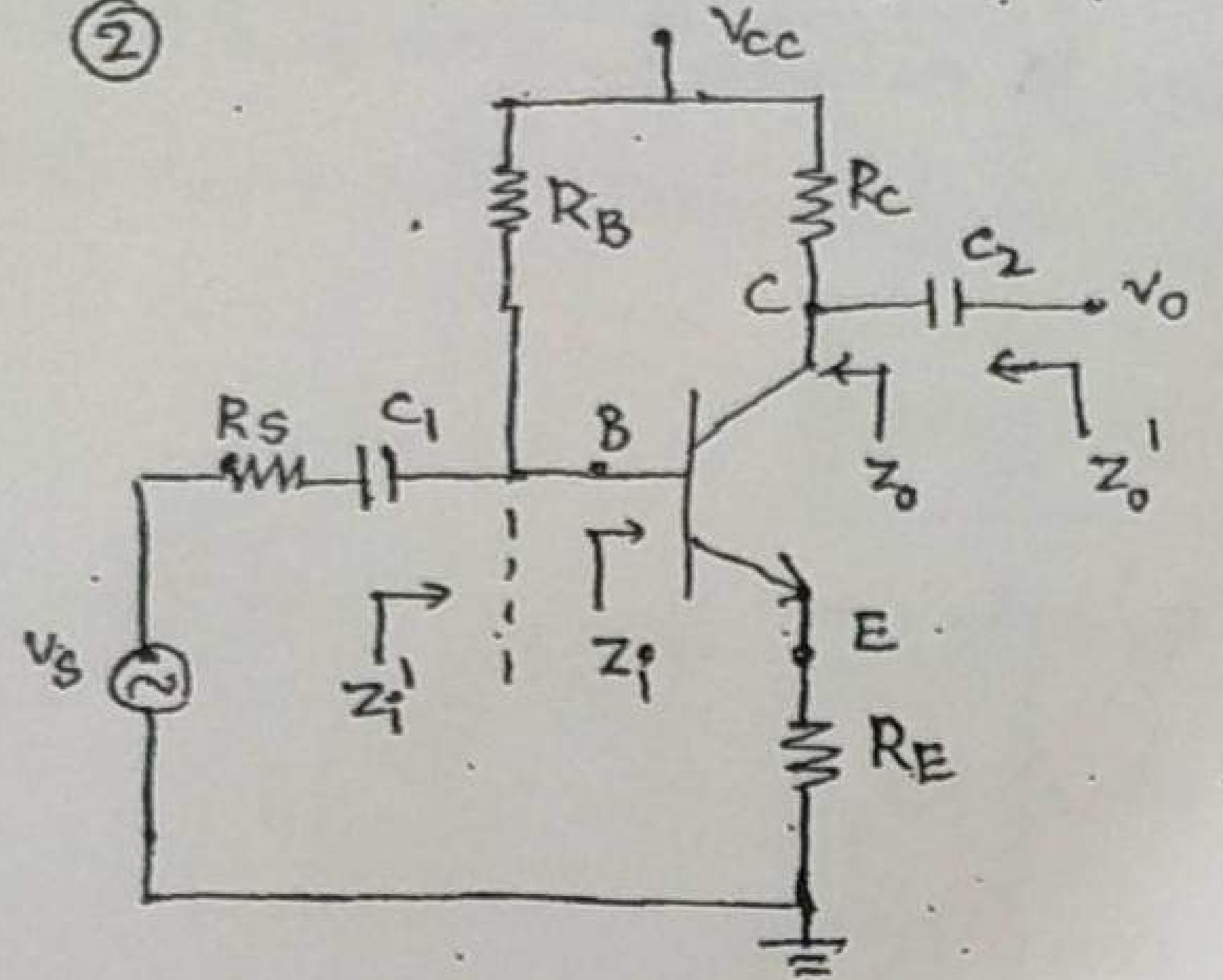
$$= \frac{R_c Z_0}{R_c + Z_0} = \frac{R_c \cancel{Z_0}}{\cancel{Z_0}(1 + \frac{R_c}{Z_0})}$$

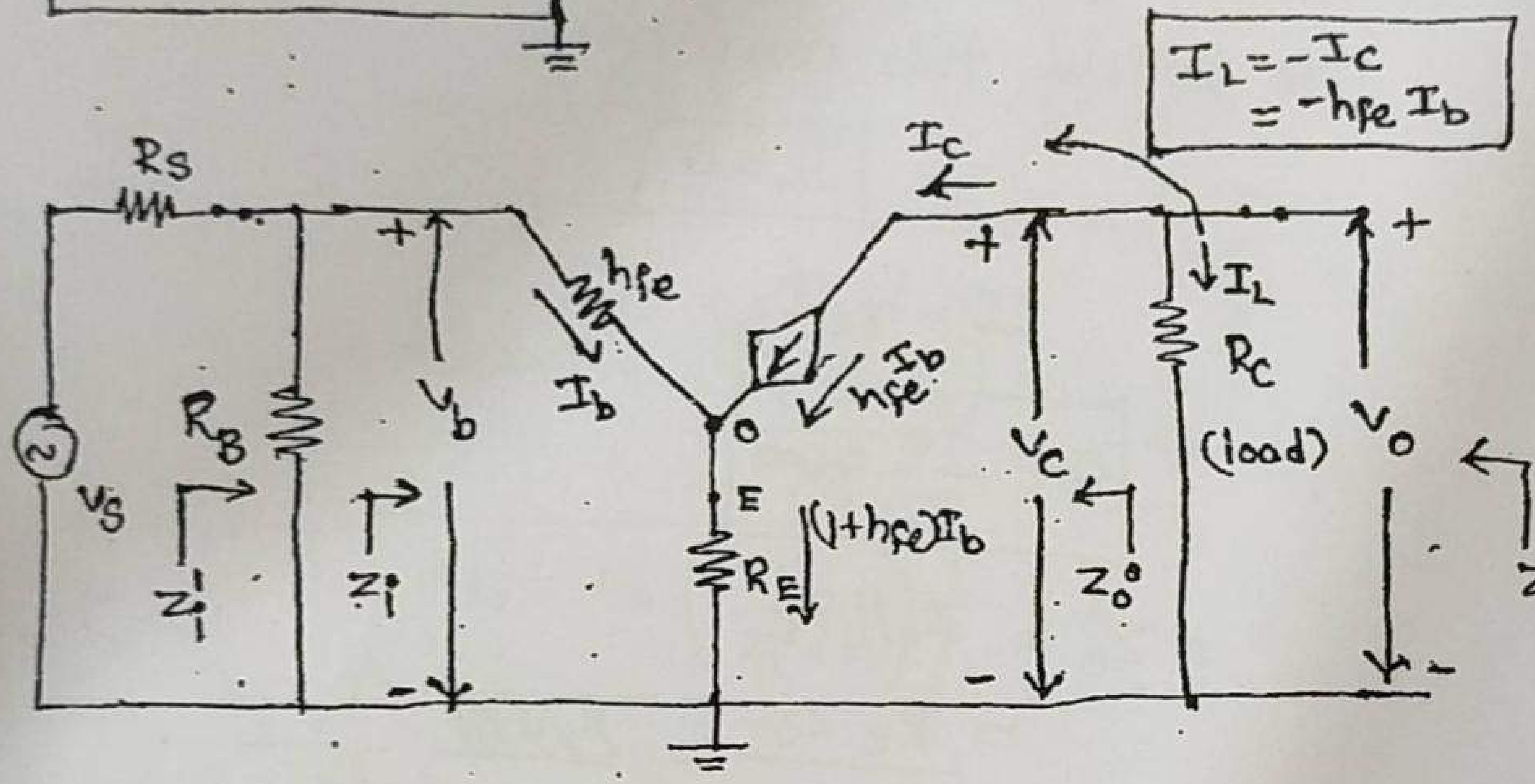
$$= \frac{R_c}{(1+0)} = R_c.$$

$$\therefore \boxed{Z_0' = R_c}.$$

* As there is no Resistor in **RE** in the above ckt its stability factor $(1+\beta)$ this ckt is thermally less sta
* To increase the thermal stability a resistor R_E connected at emitter. this resistor decreases the stability factor. and increases the thermal stability.

②





<u>Current gain</u>:-

$$A_I = \frac{I_L}{I_b} = \frac{-h_{fe} I_b}{I_b} = -h_{fe}. \qquad \boxed{A_I = -h_{fe}}$$

<u>Input impedance</u>:-

$$Z_i = \left(\frac{V_b}{I_b}\right)$$

$$V_b = h_{ie} I_b + (1+h_{fe}) I_b \cdot R_E$$

$$V_b = I_b \left[h_{ie} + (1+h_{fe}) R_E\right]$$

$$Z_i = \frac{\cancel{I_b}\left[h_{ie} + (1+h_{fe}) R_E\right]}{\cancel{I_b}}$$

$$\boxed{Z_i = h_{ie} + (1+h_{fe}) R_E}$$

$$\therefore \boxed{Z_i' = Z_i \parallel R_B}$$

Voltage gain :- $A_V = \left(\frac{V_o}{V_b}\right)$

$$V_o = I_L R_c$$

$$= -I_2 R_c = -h_{fe} I_b R_c$$

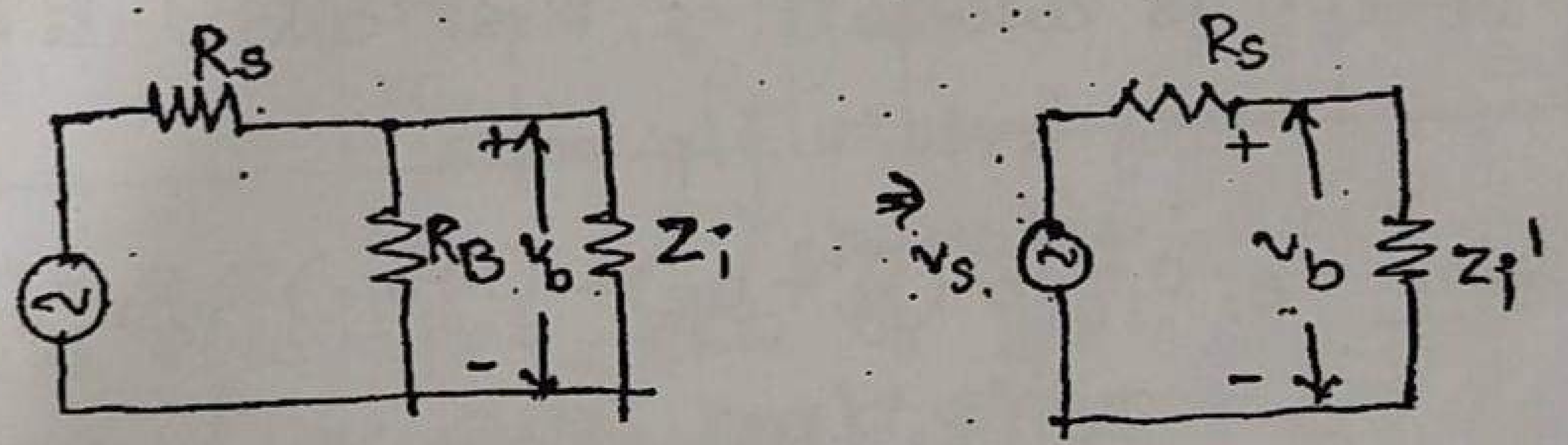
$$A_V = \frac{-h_{fe} \cancel{I_b} R_c}{\cancel{I_b}\left[h_{ie} + (1+h_{fe}) R_E\right]} = \boxed{\frac{-h_{fe} R_c}{h_{ie} + (1+h_{fe}) R_E}} \downarrow$$

dec^{n}

Voltage Amplification:-

$$A_{VS} = \frac{V_o}{V_s} = \left(\frac{V_o}{V_b}\right)\left(\frac{V_b}{V_s}\right)$$

$$A_{VS} = A_V \left(\frac{V_b}{V_S}\right)$$



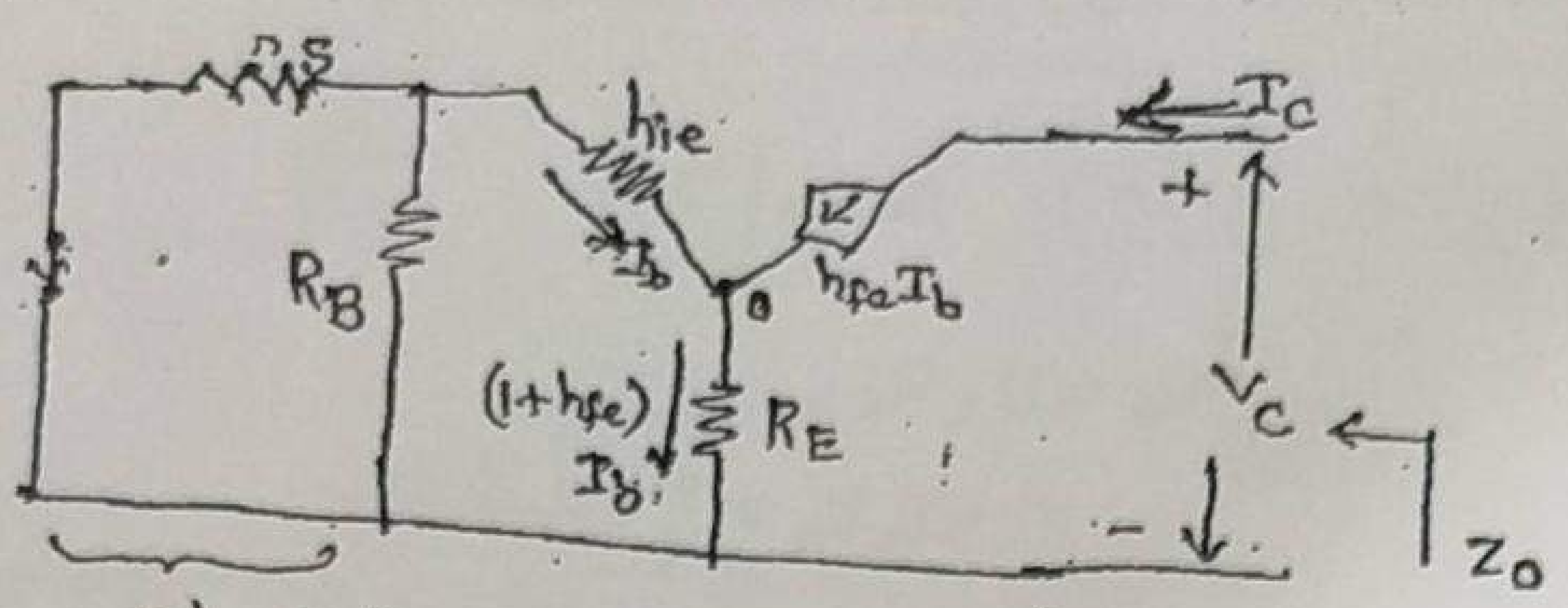
$$V_b = V_s\left(\frac{Z_i'}{Z_i' + R_s}\right)$$

$$A_{VS} = \frac{A_V \times \cancel{V_S}\left(\frac{Z_i'}{Z_i' + R_s}\right)}{\cancel{V_S}}$$

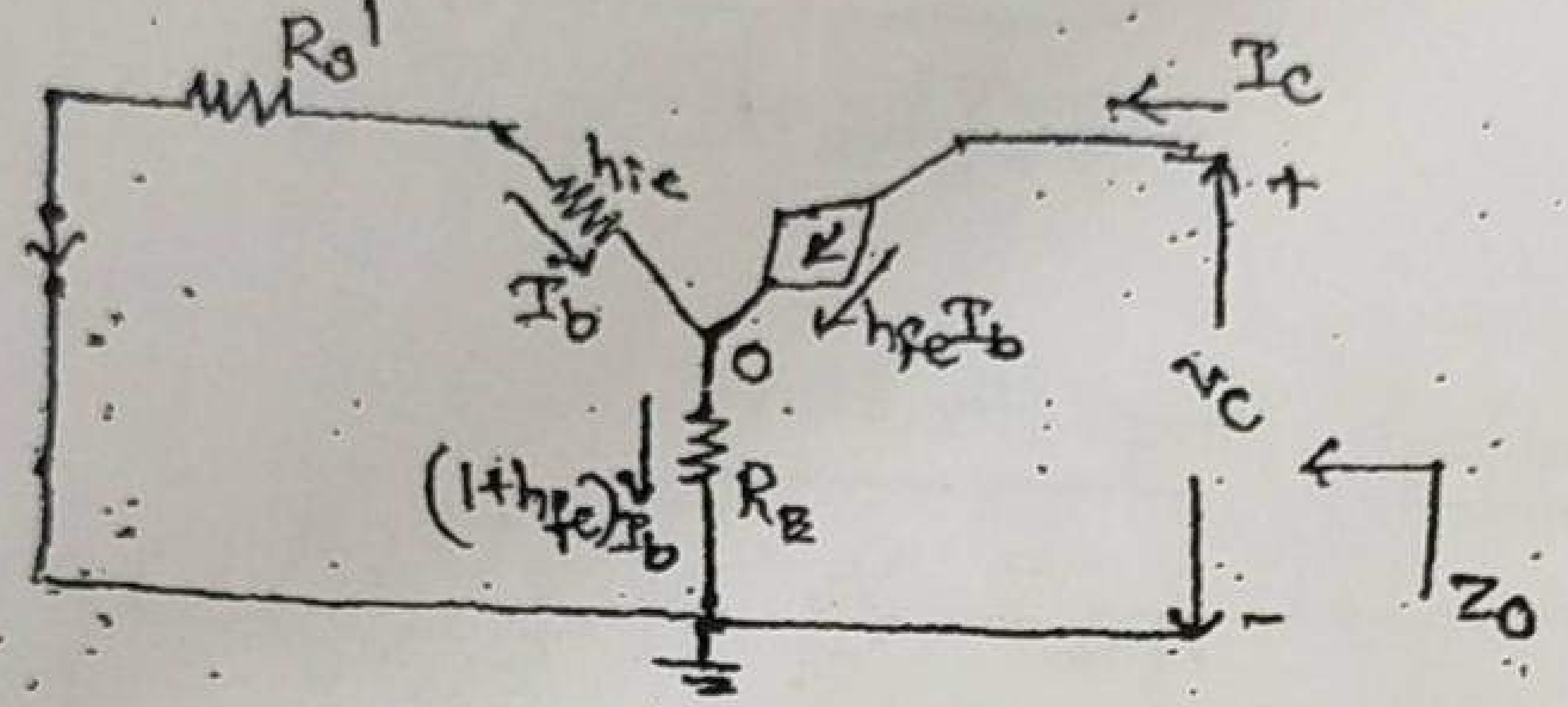
$$\boxed{A_{VS} = A_V \left(\frac{Z_i'}{Z_i' + R_s}\right)}$$

output impedance :-

$$Z_o = \left(\frac{V_c}{I_c}\right)\Bigg| \begin{array}{l} R_c \to O.C \\ V_S = 0 \end{array}$$



$R_s' = R_s // R_B$



As it is not possible to calculate v_c, go for the calculation of I_c. To calculate I_c, first calculate I_b.

Apply KVL to i/p loop.

$$0 - I_b(R_s' + h_{ie}) - (1+h_{fe}) I_b R_E = 0.$$

$$I_b\left[(R_s' + h_{ie}) + (1+h_{fe}) R_E\right] = 0$$

To satisfy this condition $\boxed{I_b = 0}$.

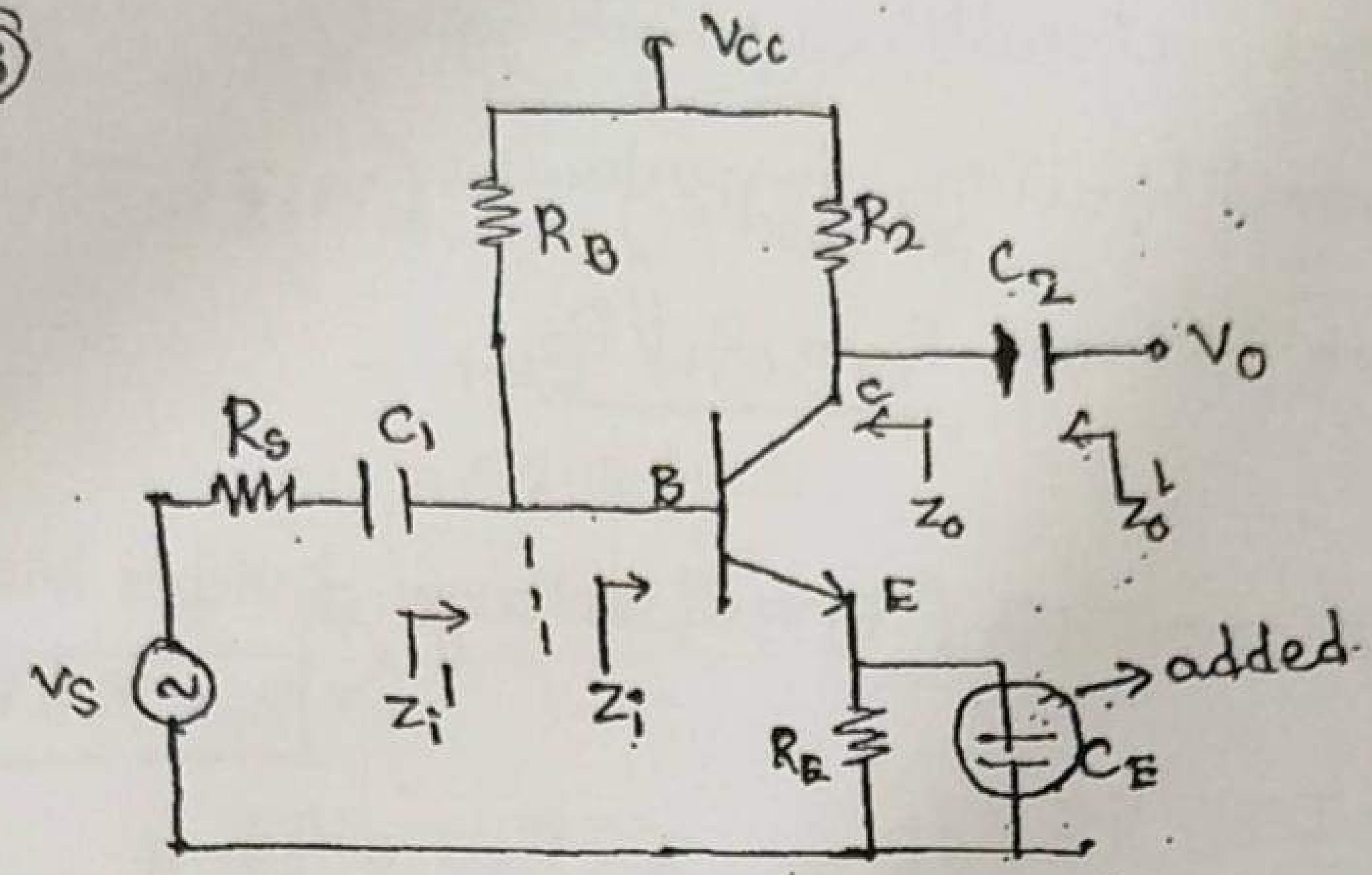
$$I_c = h_{fe} I_b = 0.$$

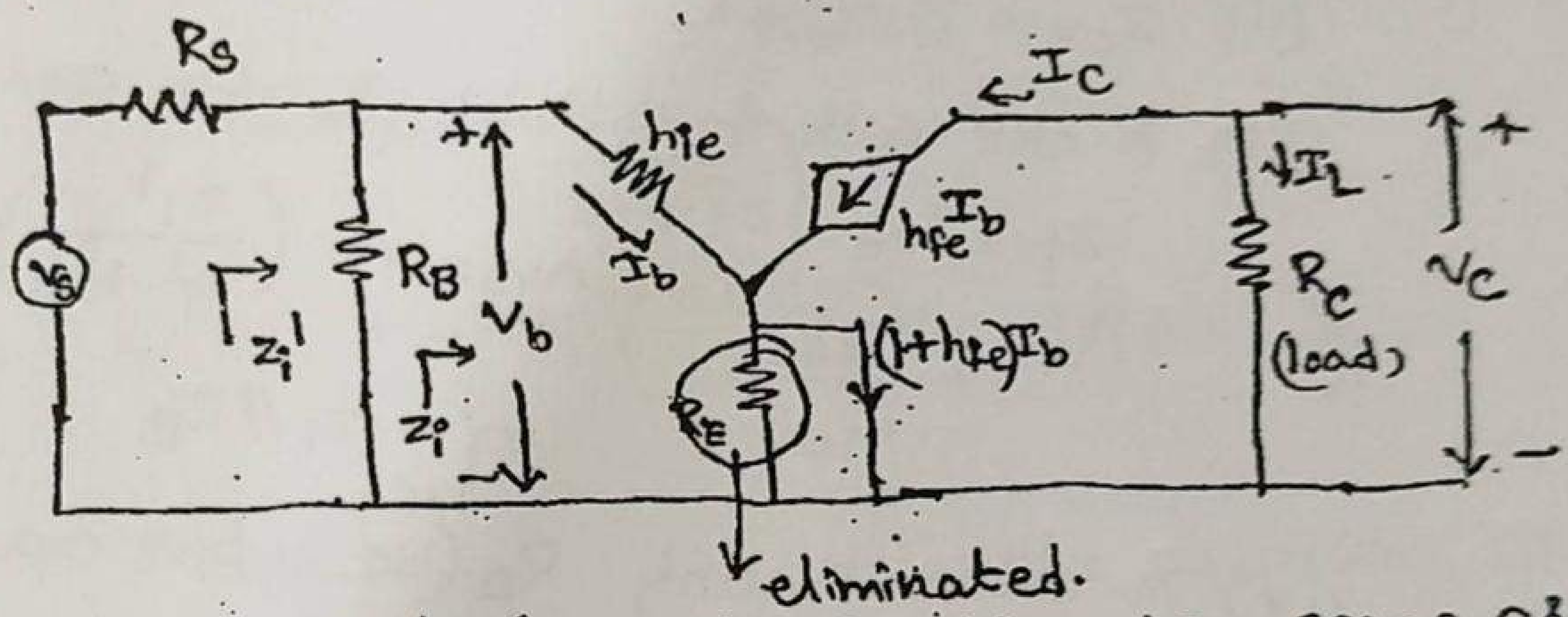
$\boxed{Z_o = \frac{v_c}{I_c} = \infty}$ $\quad Z_o' = Z_o // R_C = R_C.$

$$\boxed{Z_o' = R_C}$$

To increase the thermal stability resistor R_E connected but this resistor increases the i/p impedance (Z_i) and decreases the (A_v) value. But always we expect more voltage gain. To increase the voltage gain of the above ckt connect a capacitor across the Resistor R_E. This capacitor is called <u>By-pass capacitor</u>.

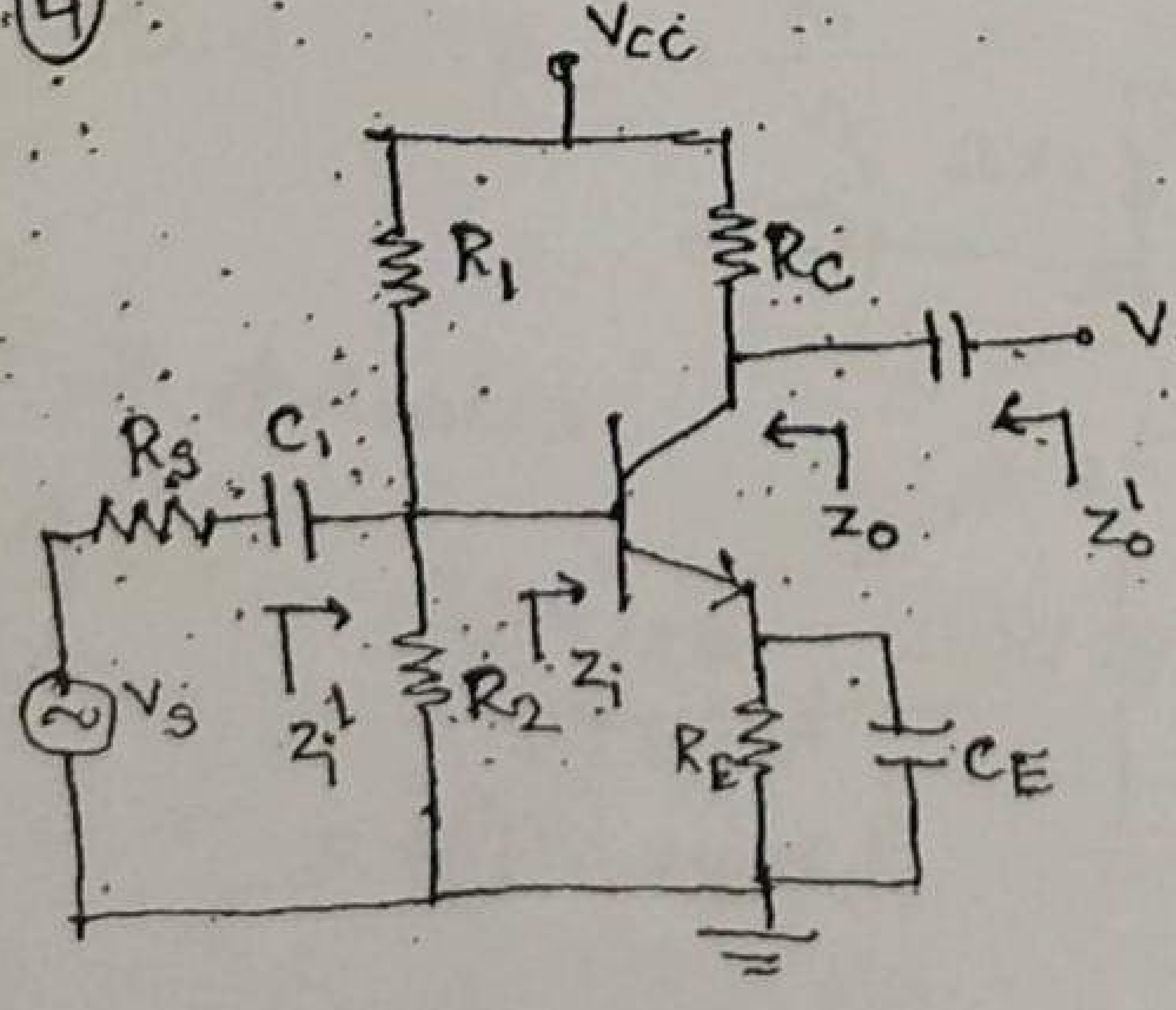
(3)



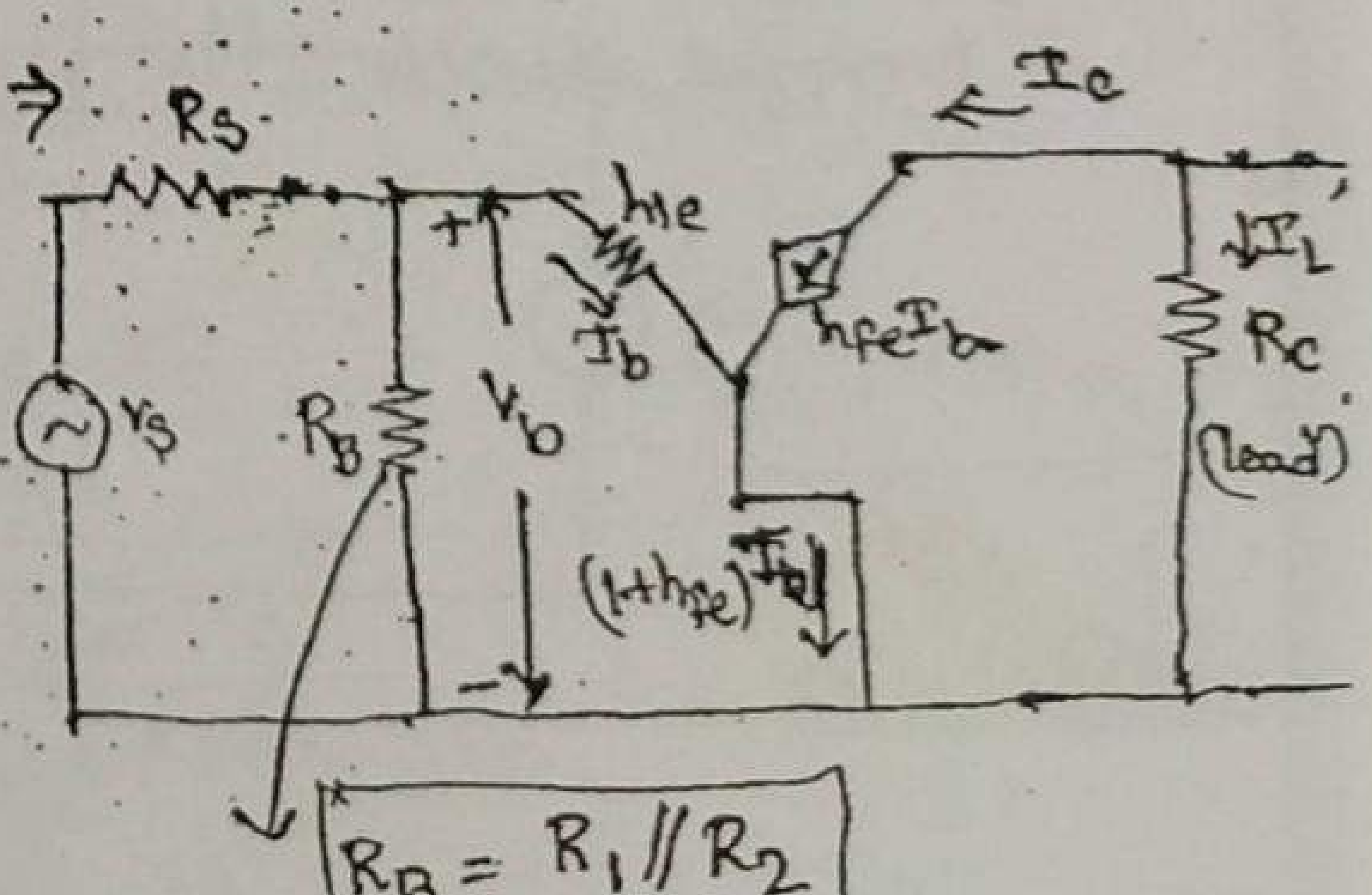


* The equivalent ckt of this is same as 1st amplifier equivalent ckt.
* "The current gain, impedances (Z_i, Z_i', Z_o, Z_o'), voltage gain, voltage amplification same as first circuit only".

(4)

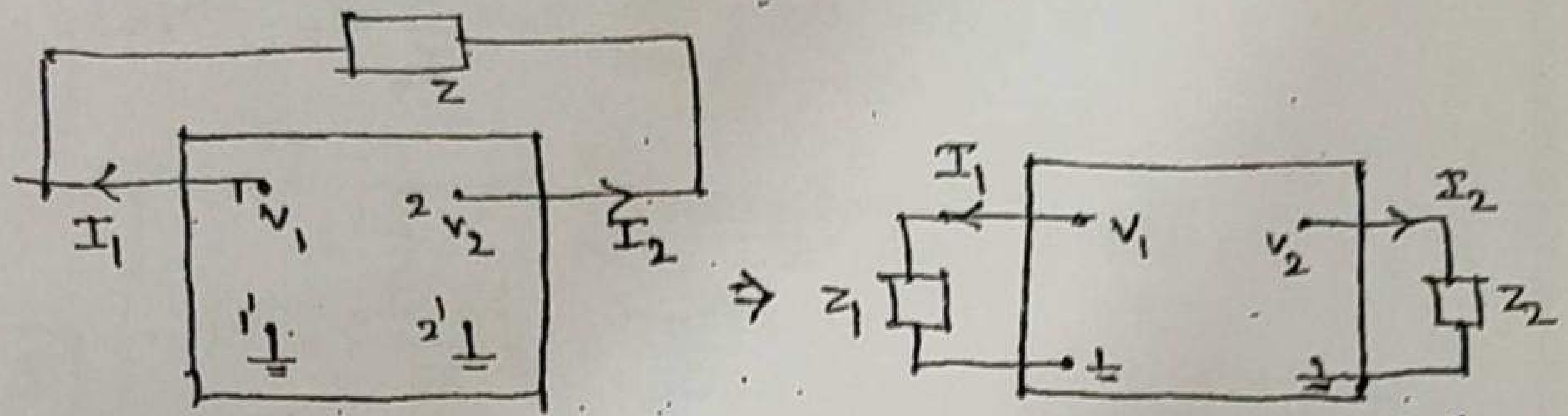


$\Rightarrow$



$\boxed{R_B = R_1 // R_2}$

Miller's theorem :-



$$I_1 = \frac{V_1 - V_2}{Z}$$

$$= \frac{1}{Z} V_1\left(1 - \frac{V_2}{V_1}\right)$$

$$I_1 = \frac{1}{Z} V_1 \, (1 - A_V)$$

$$\frac{V_1}{I_1} = \frac{Z}{1 - A_V} \Rightarrow \boxed{Z_1 = \frac{Z}{1 - A_V}}$$

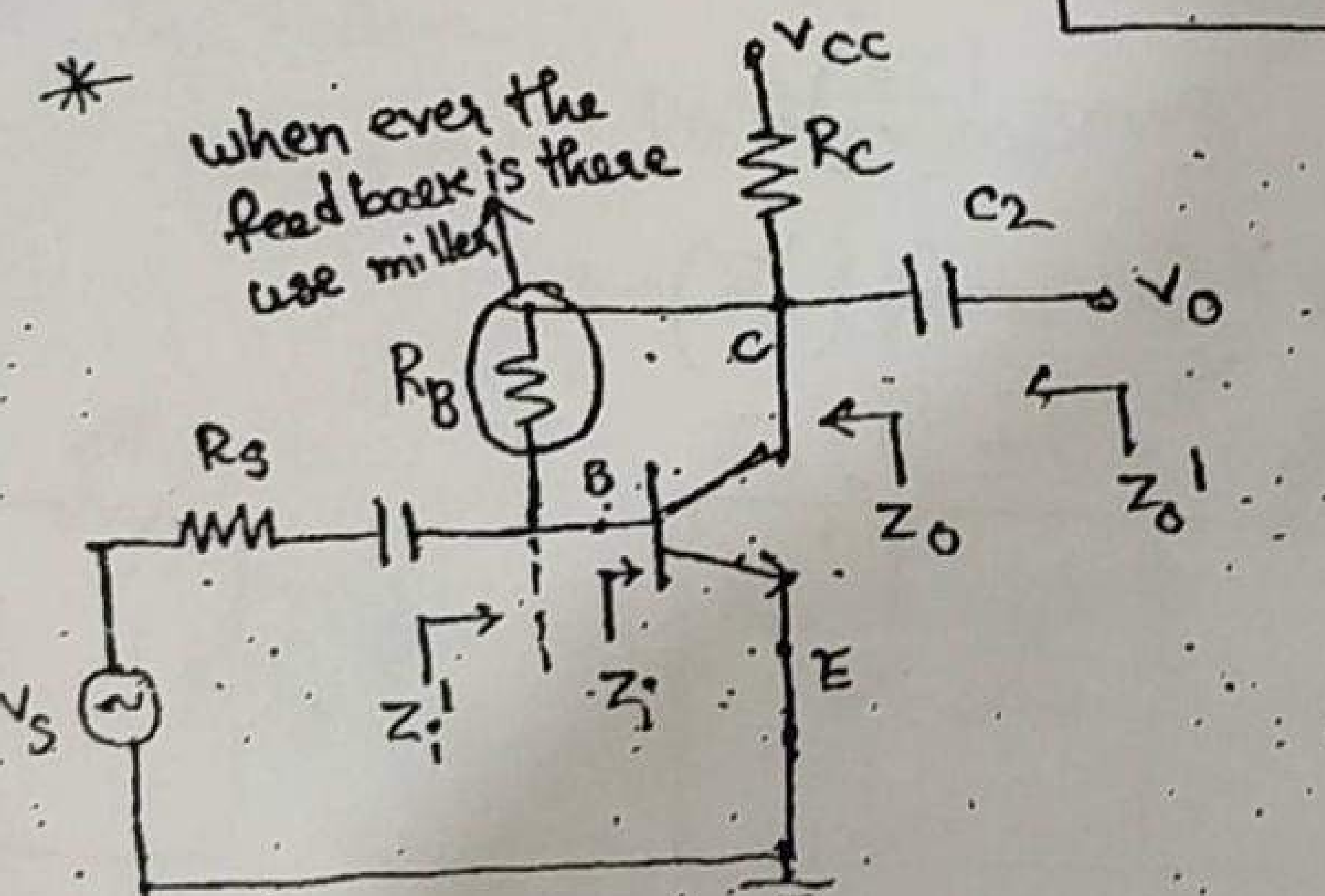
$$I_1 = \frac{V_1}{Z_1} \Rightarrow \boxed{Z_1 = \frac{V_1}{I_1}}$$

$$\boxed{Z_2 = \frac{V_2}{I_2}}$$

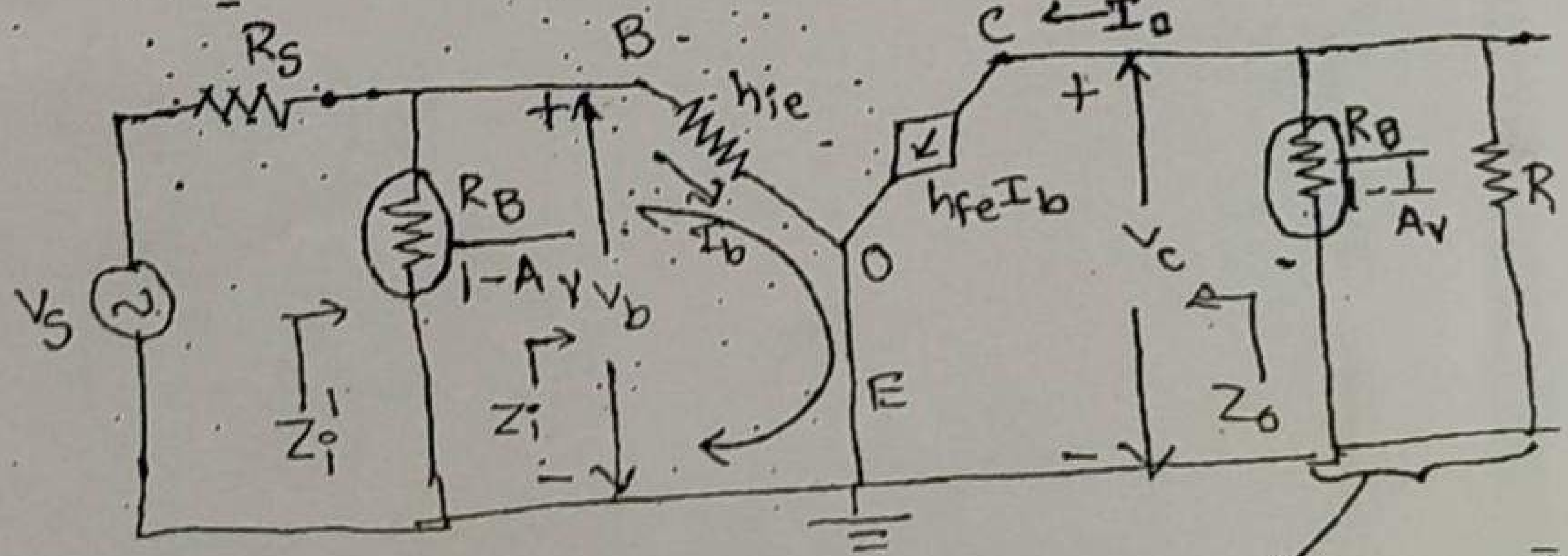
$$I_2 = \frac{V_2 - V_1}{Z} = \frac{1}{Z} V_2\left(1 - \frac{V_1}{V_2}\right) = \frac{1}{Z} V_2\left(1 - \frac{1}{A_V}\right)$$

$$\boxed{Z_2 = \frac{V_2}{I_2} = \frac{Z}{\left(1 - \frac{1}{A_V}\right)}}$$

* when ever the feed back is there use miller



$I_L = -I_c$
$= -h_{fe} I_1$



$$R_L = R_C \,//\, \frac{R_B}{1 - \frac{1}{A_V}}$$

Current gain:-

$$A_I = \frac{I_L}{I_b} = \frac{-h_{fe} I_b}{I_b} = -h_{fe}.$$

Input Impedance:-

$$Z_i = \frac{V_b}{I_b} = \frac{h_{ie} I_b}{I_b} = h_{ie}.$$

$$\boxed{Z_i = h_{ie}}$$

$$V_b - I_b h_{ie} = 0$$

$$\therefore V_b = I_b h_{ie}$$

$$\boxed{Z_i' = Z_i \,\|\, \frac{R_B}{1-A_V}}$$

Voltage gain:-

$$A_V = \frac{V_o}{V_b} = \frac{I_L R_L}{V_b}$$

$$V_o = I_L R_L$$

$$V_o = -h_{fe} I_b R_L$$

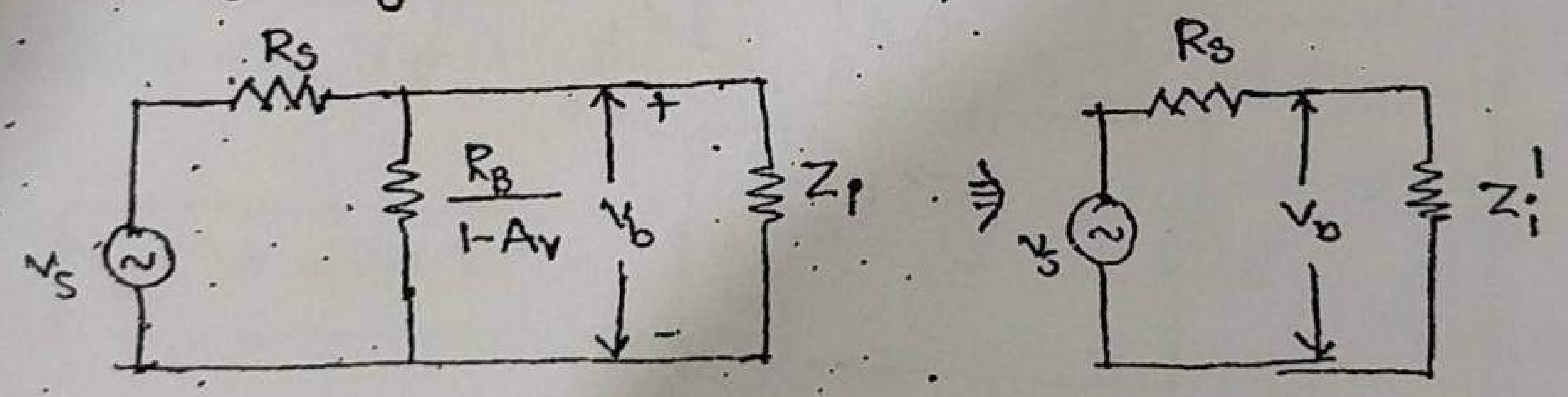
$$V_b = h_{ie} I_b$$

$$A_V = \frac{-h_{fe} I_b R_L}{h_{ie} I_b} = \frac{-h_{fe} R_L}{h_{ie}}.$$

Voltage amplification :-

$$A_{VS} = \left(\frac{V_o}{V_S}\right)$$

$$A_{VS} = \frac{V_o}{V_b} \times \frac{V_b}{V_S} = A_V\left(\frac{V_b}{V_S}\right)$$



$$V_b = V_S\left(\frac{Z_i'}{Z_i' + R_S}\right)$$

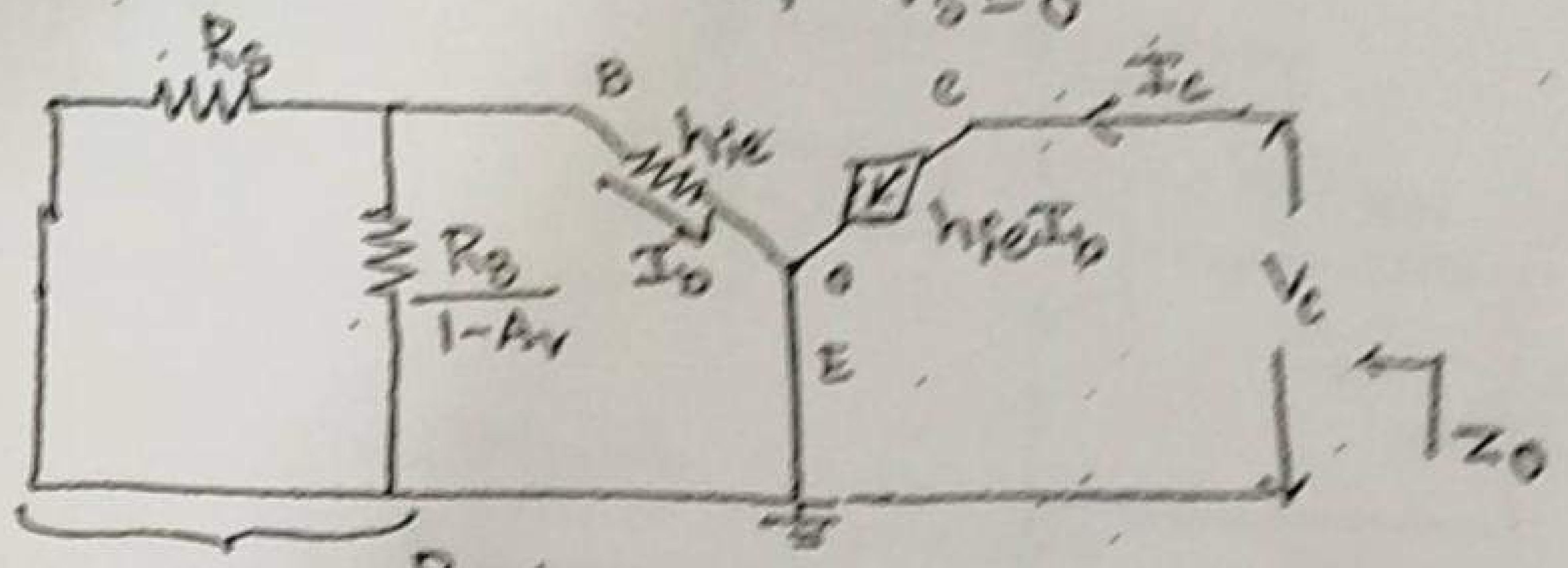
$$A_{VS} = A_V\left(\frac{\cancel{V_S}\left(\frac{Z_i'}{Z_i' + R_S}\right)}{\cancel{V_S}}\right)$$

$$A_{VS} = A_V\left(\frac{Z_i'}{Z_i' + R_S}\right)$$

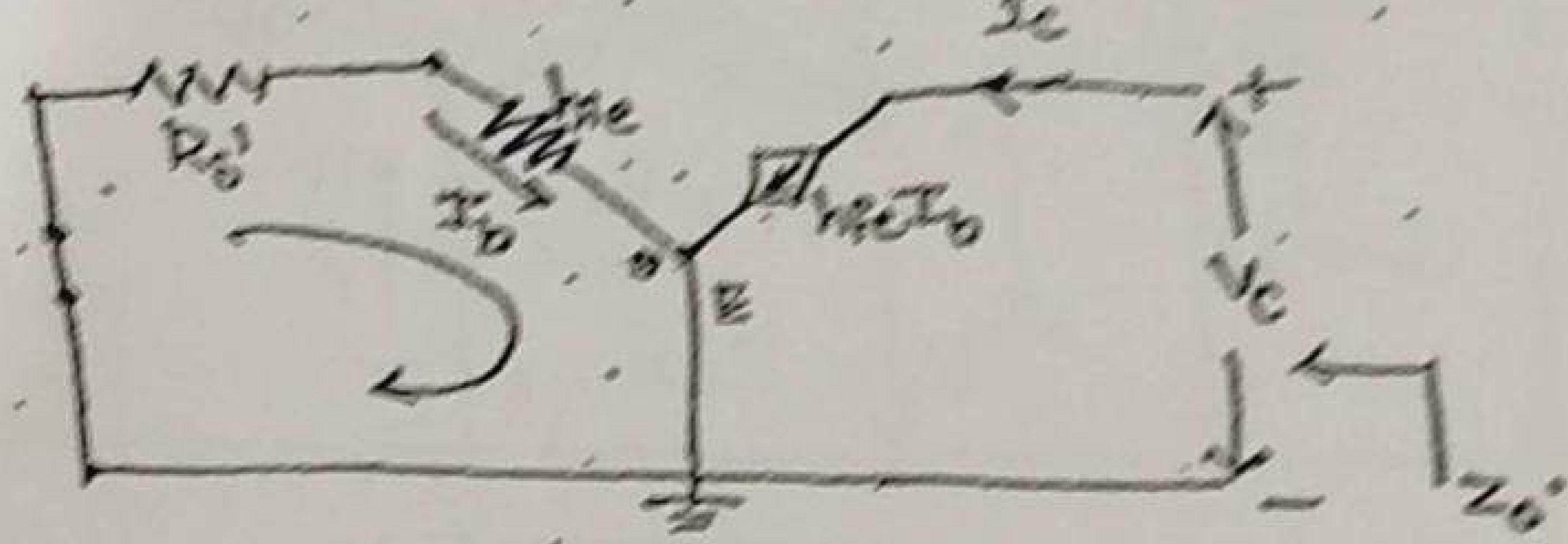
73

output impedance:-

$$Z_0 = \left. \frac{V_c}{I_c} \right| \begin{matrix} R_L \to o.c \ \& \\ V_s = 0 \end{matrix}$$



$$R_s' = R_s // \frac{R_B}{1-A_v}$$



As it is not possible to calculate V_c go for the calculation of I_c. To calculate I_c first calculate I_b value.

Apply KVL to i/p loop.

$$0 - I_b(R_s' + h_{ie}) = 0$$

$$I_b(R_s' + h_{ie}) = 0$$

To satisfy this condition,

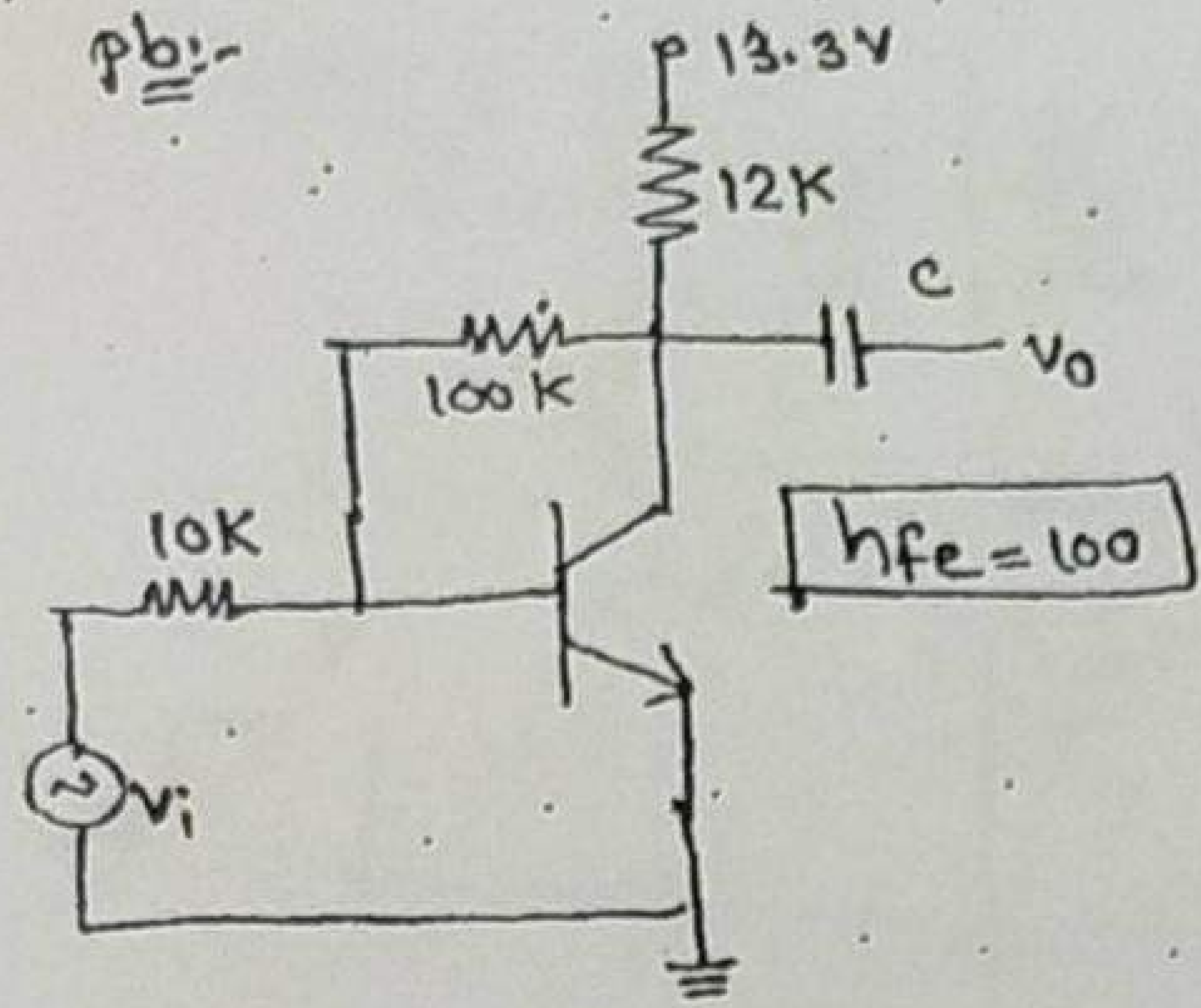
$$I_b = 0$$

$$I_c = h_{fe} I_b = 0$$

$$Z_0 = \frac{V_c}{I_c} = \infty$$

$$Z_0' = R_L // Z_0 \Rightarrow \boxed{Z_0' = R_L}$$

pb:-



for the amplifier ckt shown, Calculate the gain $\frac{V_0}{V_I} = ?$

Sol: Assume $\boxed{h_{ie} = 1.1K\Omega}$

$$A_I = -h_{fe} = -100$$

$$Z_i = h_{ie} = 1.1K\Omega$$

$$R_L = R_C \parallel \frac{R_B}{1 - \frac{1}{A_V}}$$

$$\Rightarrow \boxed{A_V = \frac{-h_{fe}R_L}{h_{ie}}}$$

The voltage gain A_V of CE is assumed to be very high

$\frac{1}{A_V} \rightarrow$ very low

$$\Rightarrow 1 - \frac{1}{A_V} \simeq 1$$

$$\therefore R_L = R_C \parallel R_B$$

$$= \frac{12K \times 100K}{112} = 10.71K\Omega$$

$$A_V = -\frac{h_{fe} R_L}{h_{ie}}$$

$$= \frac{-100 \times 10.71}{1.1} = -973.63$$

$$Z_i' = Z_i \parallel \frac{R_B}{1 - A_V}$$

$$\frac{R_B}{1 - A_V} = \frac{100 \times 10^3}{974.63} = 102.60\Omega$$

$$* \; Z_i' = \frac{1100 \times 102.60}{1202.60}$$

$$= 93.84\Omega$$

$$A = \frac{V_0}{V_i}$$

$$= A_V \left(\frac{Z_i'}{Z_i' + R_s} \right)$$

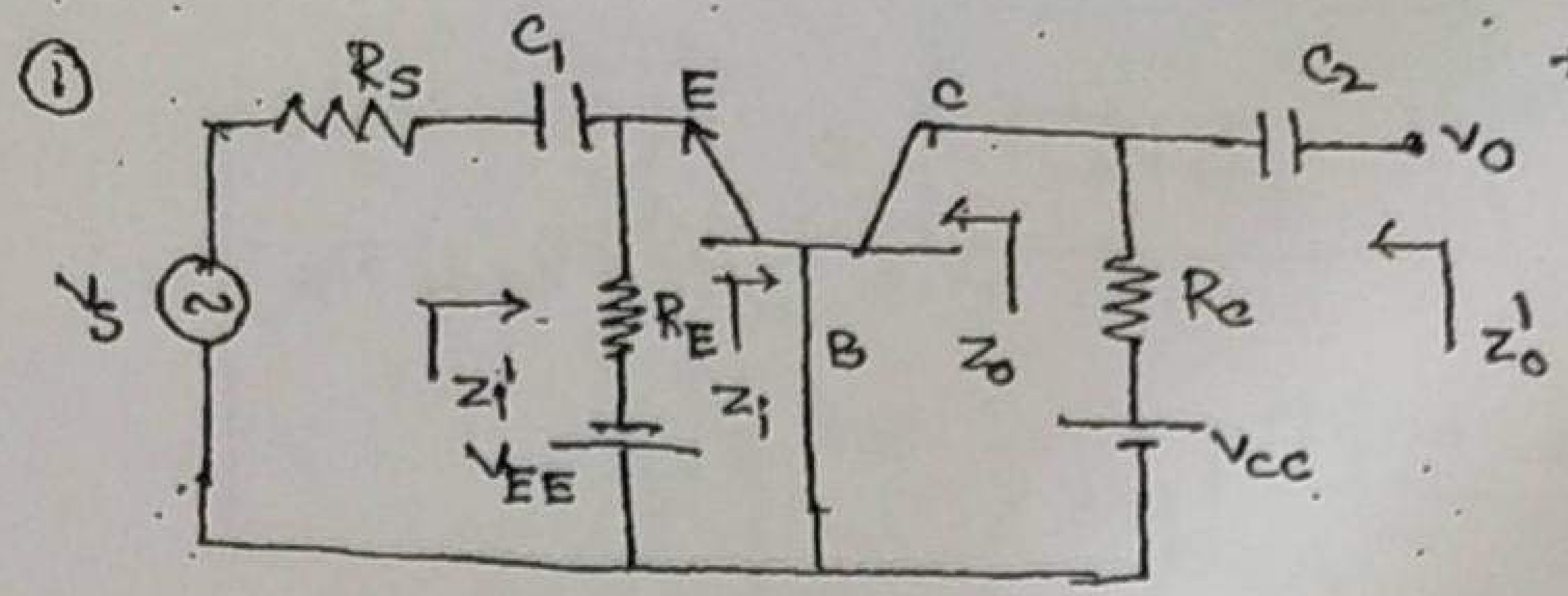
$$= -973.63 \left(\frac{93.84}{93.84 + 10^4} \right)$$

$$A = -9.05$$

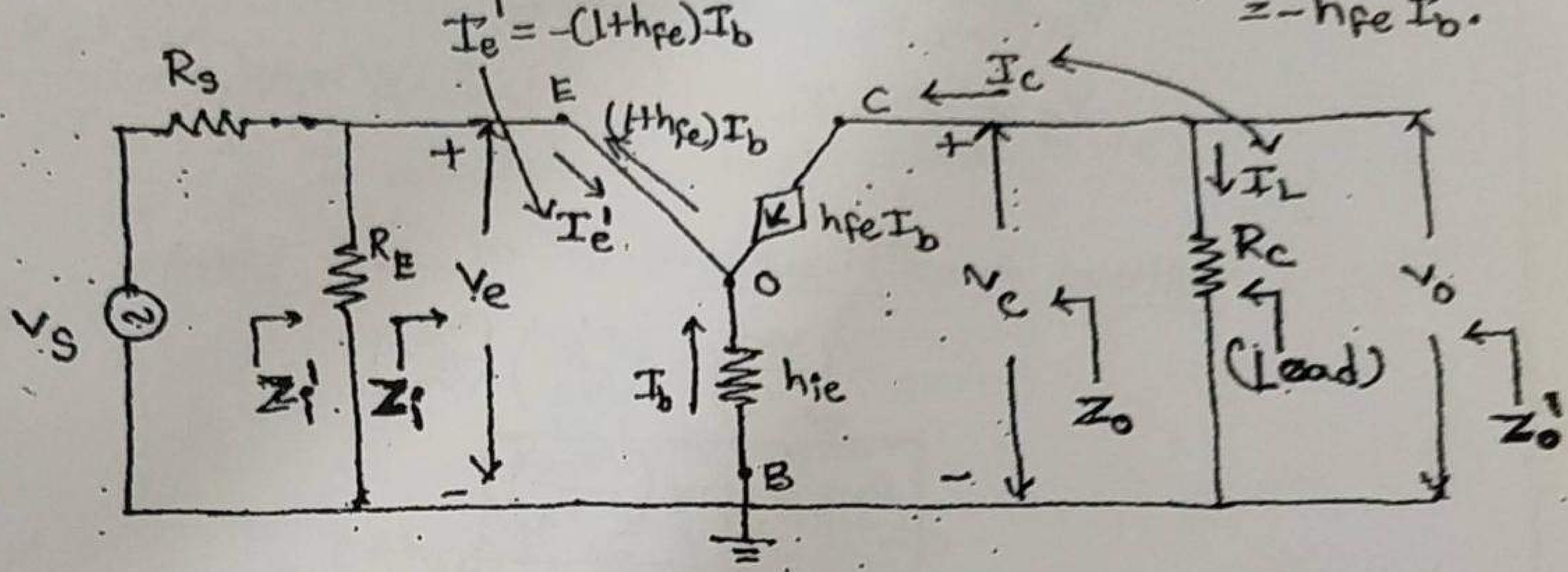
$$\boxed{A \simeq 10}$$

** * CB Amplifier:-

(i)



$I_L = -I_c$
$= -h_{fe} I_b$.



1. current gain:-

$$A_I = \left(\frac{I_L}{I_e'}\right) = \frac{-h_{fe} I_b}{-(1+h_{fe}) I_b} = \frac{h_{fe}}{(1+h_{fe})}.$$

As $D_r > N_r \Rightarrow \boxed{A_I < 1}$. But

$h_{fe} \ggg 1 \Rightarrow A_I \simeq 1$

The o/p current $\simeq$ i/p current.

* The o/p current follows the i/p current.
* The ckt is current follower (or) current Buffer

$\therefore$ The CB Amplifier used as a current Buffer ckt.

2. Input impedance:-

$$Z_i = \frac{V_e}{I_e'}$$

$V_e = -h_{ie} I_b \quad \Rightarrow Z_i = \frac{-h_{ie} I_b}{-(1+h_{fe}) I_b} = \frac{h_{ie}}{(1+h_{fe})}$

$$\Rightarrow \boxed{Z_i = \frac{h_{ie}}{1+h_{fe}}} \quad \Rightarrow Z_i \text{ is very low}$$

$$Z_i' = Z_i \,//\, R_E.$$

Voltage gain:-

$$A_V = \left(\frac{V_o}{V_e}\right)$$

$$V_o = I_L R_C = -h_{fe} I_b R_C$$

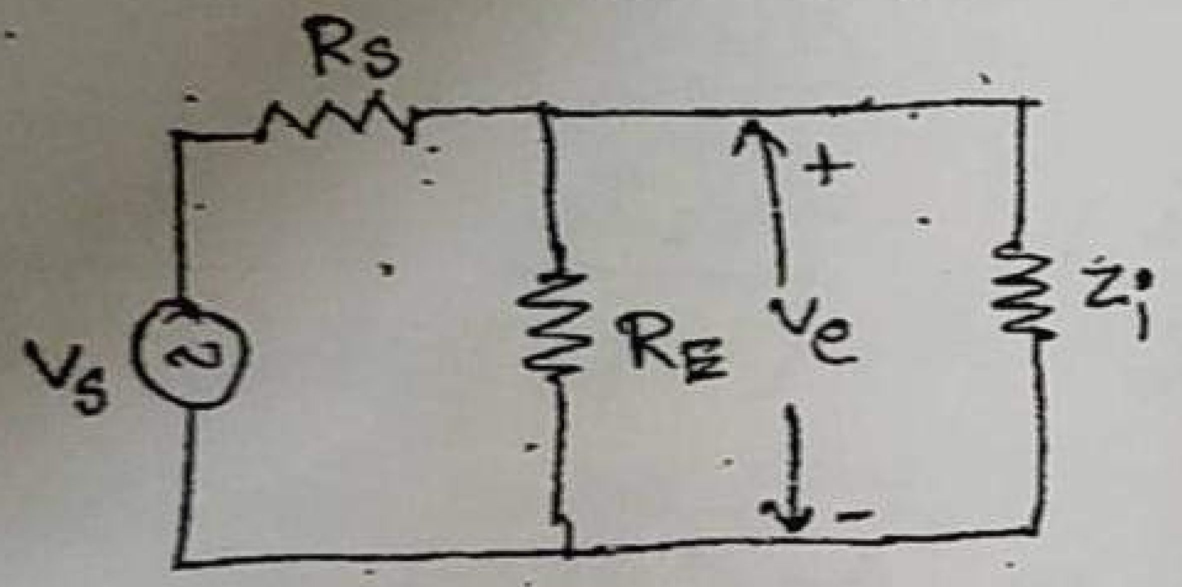
$$V_e = -h_{ie} I_b$$

$$\therefore A_V = \frac{\cancel{-}h_{fe} I_b R_C}{\cancel{-}h_{ie} I_b} = \left(\frac{h_{fe} R_C}{h_{ie}}\right)$$

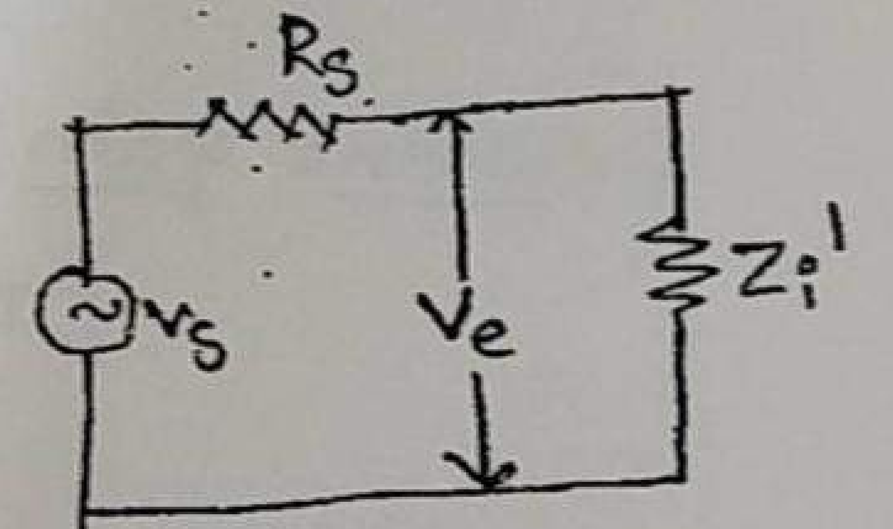
Voltage Amplification:-

$$A_{VS} = \left(\frac{V_o}{V_s}\right) = \left(\frac{V_o}{V_e}\right)\left(\frac{V_e}{V_s}\right)$$

$$\boxed{A_{VS} = A_V \left(\frac{V_e}{V_s}\right)}$$



$\Rightarrow$



$$V_e = V_s\left(\frac{Z_i'}{Z_i' + R_s}\right)$$

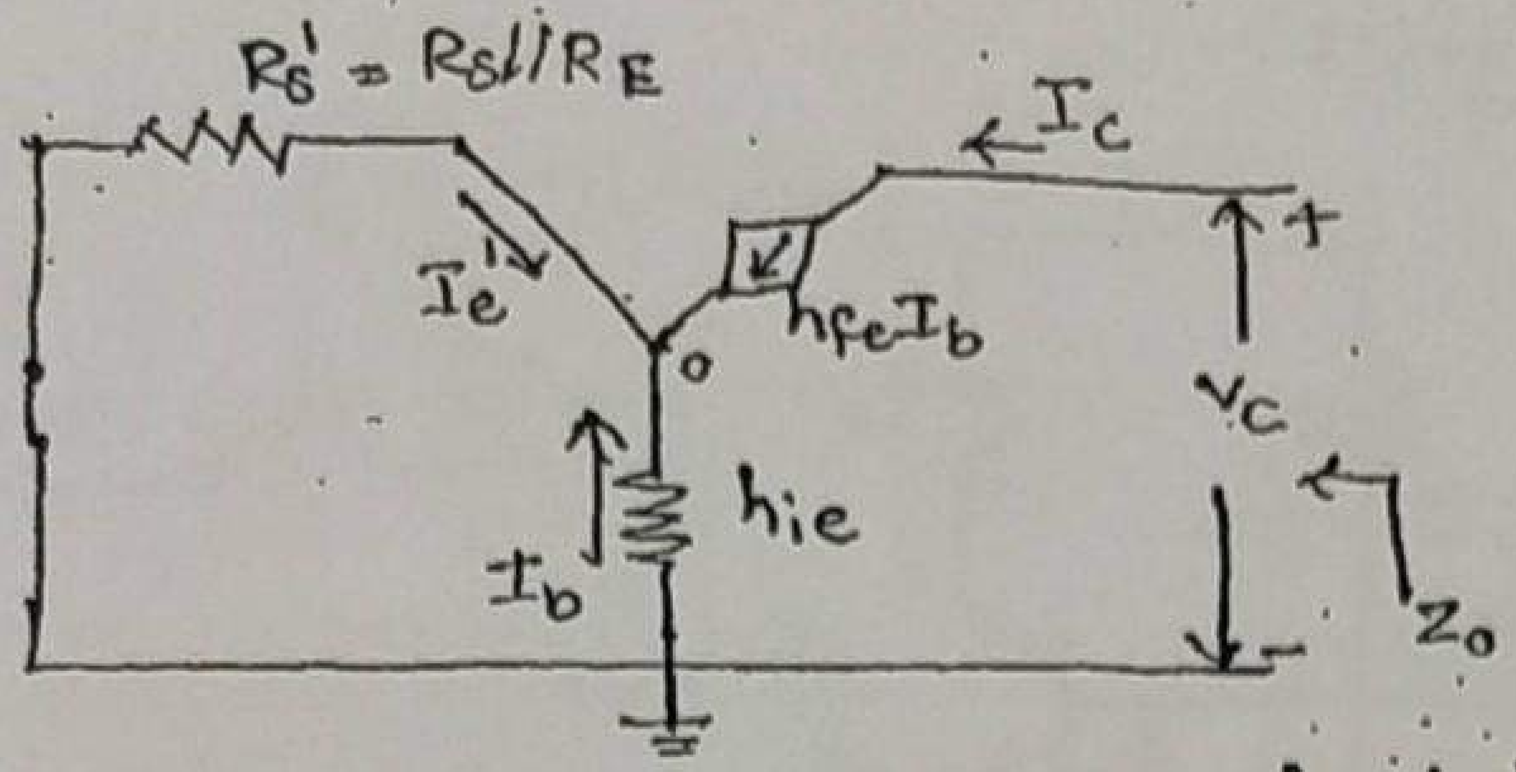
$$A_{VS} = A_V \left[\frac{\cancel{V_s}\left(\frac{Z_i'}{Z_i'+R_s}\right)}{\cancel{V_s}}\right] \Rightarrow \boxed{A_{VS} = A_V \left[\frac{Z_i'}{Z_i' + R_s}\right]}$$

As $R_s >\!>\!> Z_i'$ $\Rightarrow A_{VS} << A_V$.

(A_{VS} is very low for CB Amp) $\therefore$ The CB Amp. cannot be used for voltage Amplification.

Output impedance (Z_o):-

$$Z_o = \left(\frac{V_c}{I_c}\right) \Bigg|\, \begin{matrix} R_C \to O.C \\ \& \\ V_s = 0. \end{matrix}$$



As it is not possible to calculate V_c, so for the calculation of I_c.

To calculate I_c, first calculate I_b.

Apply KVL to i/p loop :

$$0 - I_e' R_s' - h_{ie}(-I_b) = 0$$

$$-I_e' R_s' + h_{ie} I_b = 0$$

$$(1+h_{fe}) I_b R_s' + h_{ie} I_b = 0$$

$$I_b((1+h_{fe})R_s' + h_{ie}) = 0$$

To satisfy the condition.

$$I_b = 0.$$

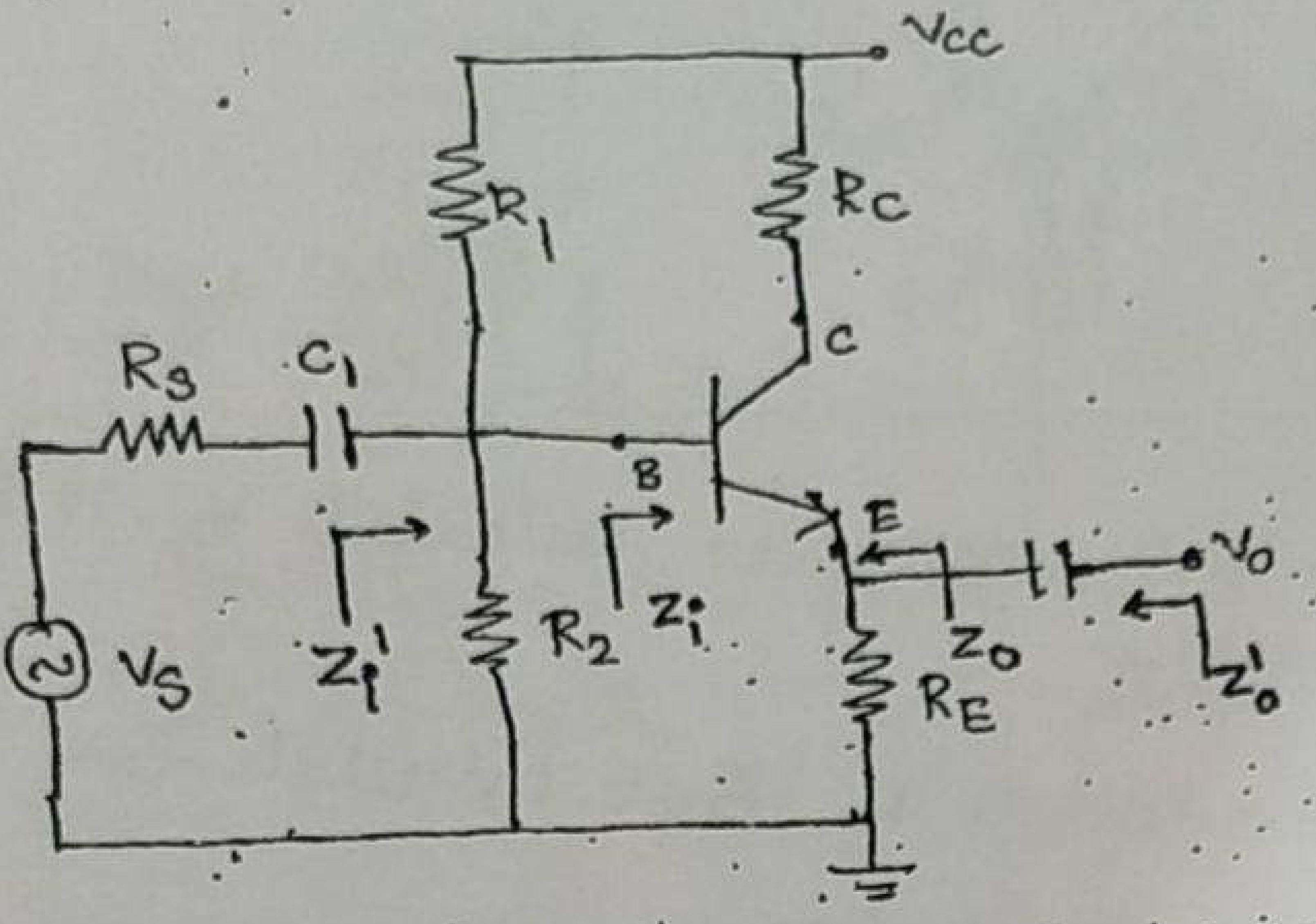
$$I_c = h_{fe} I_b = 0$$

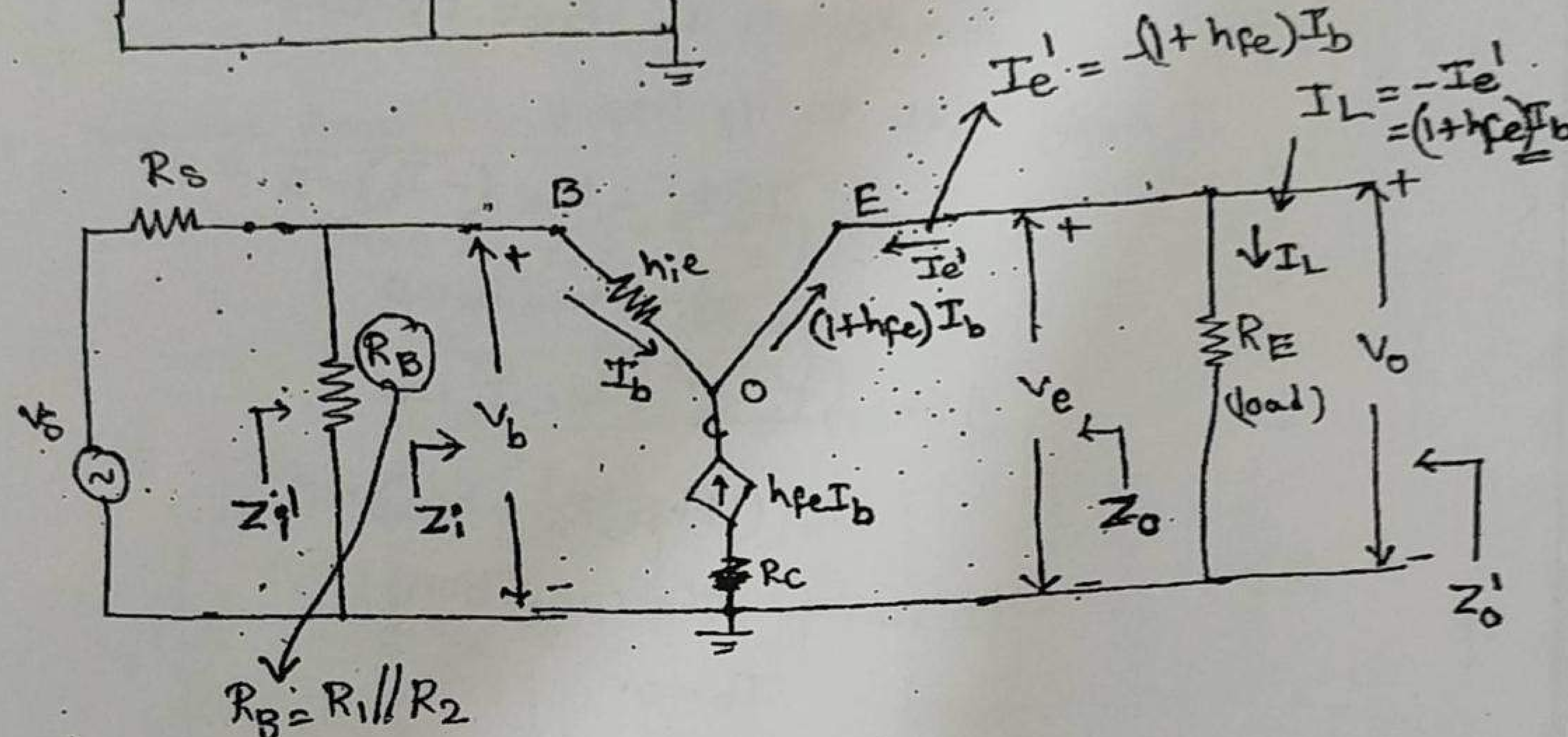
$$Z_o = \frac{V_c}{I_c} = \infty$$

$$Z_o' = R_c // Z_o = \underline{\underline{R_c}}$$

* CB Amplifier can't used for voltage amplification & current amplifion. It is only used for o/p current ≃ i/p current.

→ CC Amplifier :-

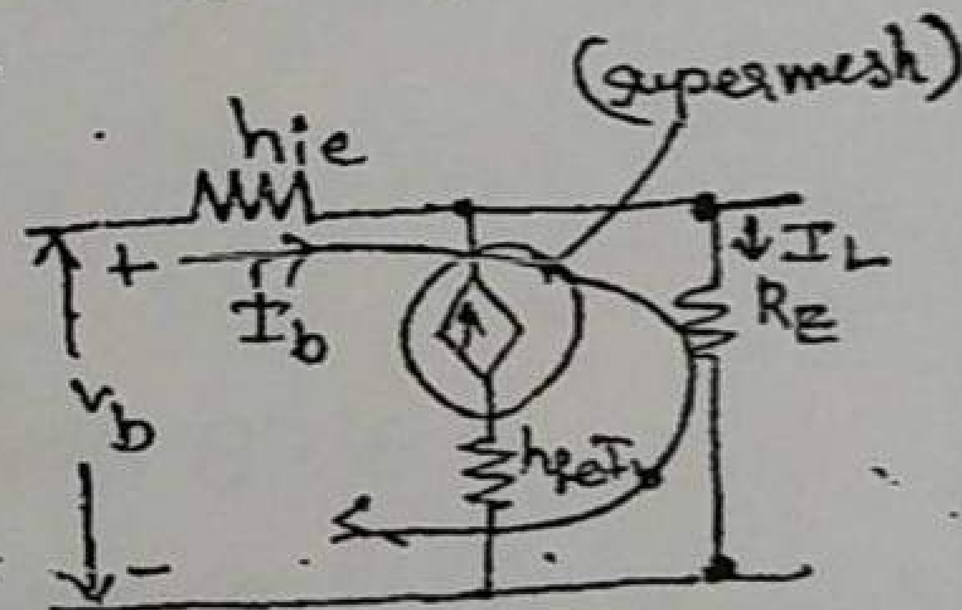




current gain :-

$$A_I = \frac{I_L}{I_b} = \frac{(1+h_{fe})\, I_b}{I_b} = (1+h_{fe}).$$

Input impedance :-



$$Z_i = \left(\frac{V_b}{I_b}\right) =$$

$$\cancel{V_b = h_{ie} I_b - h_{fe} I_b \cdot R_C}$$

$$V_b = h_{ie} I_b + I_L R_E$$

$$= h_{ie} I_b + (1+h_{fe}) I_b \cdot R_E$$

$$V_b = I_b \left(h_{ie} + (1+h_{fe}) R_E \right)$$

$$Z_i = \frac{V_b}{I_b} = \frac{I_b \left(h_{ie} + (1+h_{fe}) R_E\right)}{I_b} = h_{ie} + (1+h_{fe}) R_E \, ;$$

$$Z_i' = Z_i \parallel R_B.$$

<u>voltage gain (A_V)</u> $= \dfrac{V_o}{V_b}$:-

$V_o = I_L R_E.$

$\therefore V_o = (1+h_{fe}) I_b R_E.$

$$A_V = \frac{V_o}{V_b}$$

$$A_V = \frac{(1+h_{fe})\cancel{I_b} R_E}{\cancel{I_b}[h_{ie} + (1+h_{fe})R_E]}$$

$$\boxed{A_V = \frac{(1+h_{fe})R_E}{h_{ie}+(1+h_{fe})R_E}}$$

As $N_r < D_r$, $A_V < 1$.

if $(1+h_{fe})R_E >>> h_{ie}$ $\therefore \boxed{A_V \simeq 1}$

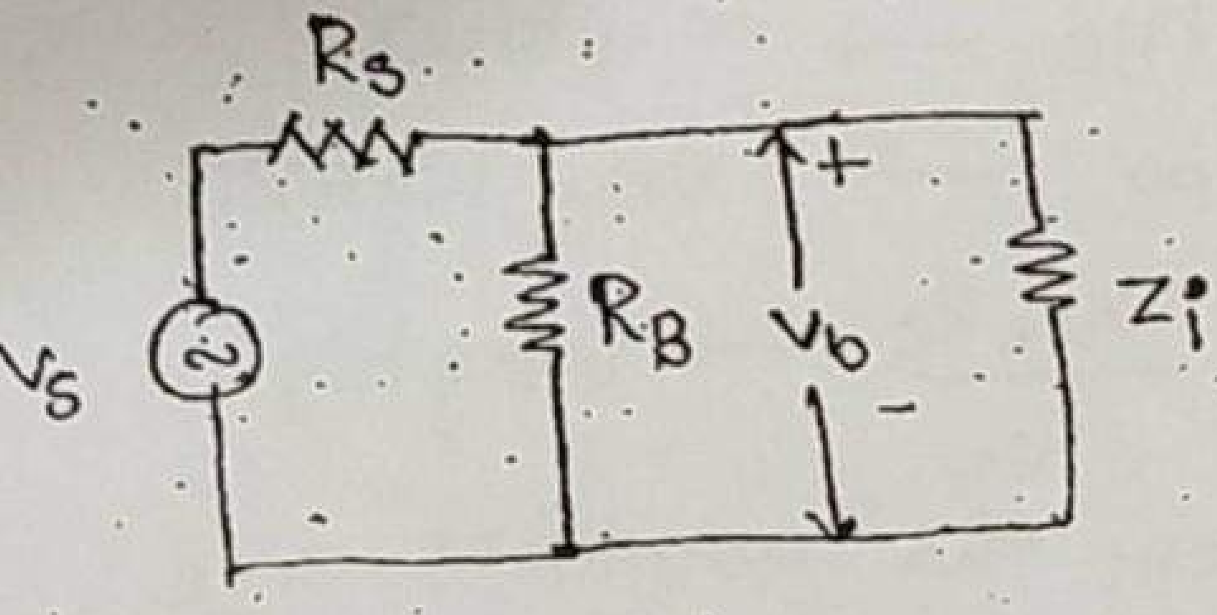
The o/p voltage follows the i/p voltage.

$\rightarrow$ voltage follower ckt (OR)
voltage Buffer ckt (or)
Emitter follower ckt

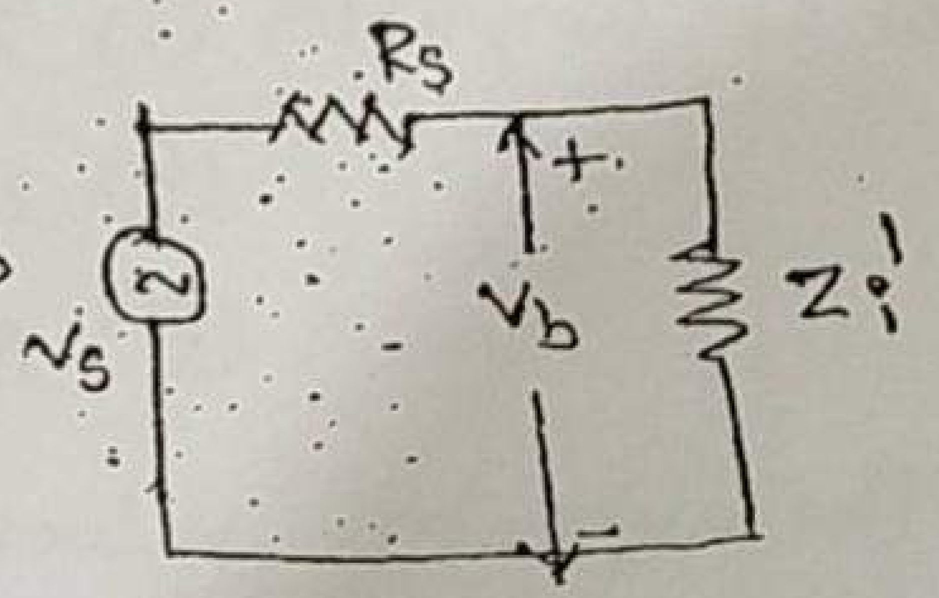
* cc Amplifier used as voltage Buffer ckt..

<u>voltage Amplification</u>:-

$$A_{VS} = \frac{V_o}{V_S} = \left(\frac{V_o}{V_b}\right)\left(\frac{V_b}{V_S}\right) \Rightarrow A_{VS} = A_V\left(\frac{V_b}{V_S}\right)$$



$\Rightarrow$



$$V_b = V_S\left(\frac{Z_i'}{Z_i' + R_S}\right)$$

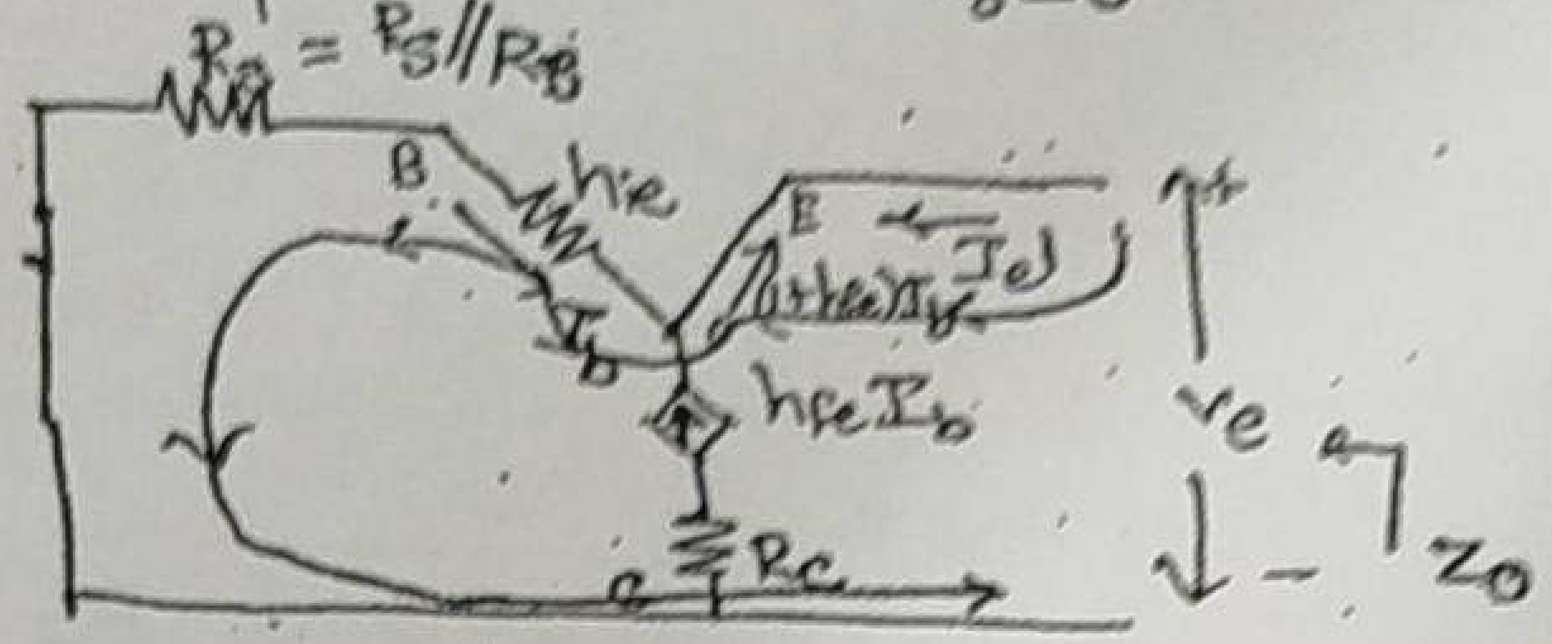
$$A_{VS} = A_V\left(\frac{V_b}{V_S}\right) = A_V\left(\frac{Z_i'}{Z_i' + R_S}\right).$$

$\frac{-1}{Z_i^1 + R_s} < 1$ (or) $A_v < 1 \Rightarrow A_{vs} < 1$

∴ CC Amplifier cannot be used for voltage amplification

<u>output impedance (Z_o):-</u>

$$Z_o = \frac{V_e}{I_e^1} \Bigg| \begin{array}{l} R_E \rightarrow o.c \\ \& \\ V_s = 0 \end{array}$$



$V_e = -I_b(h_{ie} + R_s^1)$

$I_e^1 = -(1+h_{fe}) I_b$. ∴ $Z_o = \frac{+I_b(h_{ie} + R_s^1)}{+(1+h_{fe})I_b}$

$Z_o \rightarrow$ very low for cc amplifier

$$\boxed{Z_o = \frac{h_{ie} + R_s^1}{1+h_{fe}}}$$

$$\boxed{Z_o^1 = Z_o // R_E}$$

<u>For CE amplifier :-</u>

* Among these '3' the CE is only used for amplification.
* For CE amplifier is most preferable ~~to~~ be used amplifier.
* for CE amplifier (i) $Z_i = h_{ie} \longrightarrow$ very low.
  (ii) $Z_o = \infty \longrightarrow$ very high.
  (iii) $A_v = \frac{-h_{fe} R_c}{h_{ie}} \longrightarrow$ very high.

The expected values from the amplifier are

(i) $A_v \rightarrow$ very high - (more amplification).

(ii) $Z_i \rightarrow$ very high - ↑ driving capacity of ckt &
- power dissipation in the
... is less.

(iii) Z_0 - Very low - ↓ the loading effect on i/p signal.

* As we compare the CE amplifier values with the expected values from the amplifier the CE amplifier not satisfying the impedance chara So there is a necessity to improve the Impe ance characteristics (↑ i/p impedance, ↓ o/p impedance

* As the collector collecting the charged particles, the temperature across the junction J_c increases.

As T↑ ⇒ h_{fe}↑, A_v↑ but the gain of amplifier must be constant.

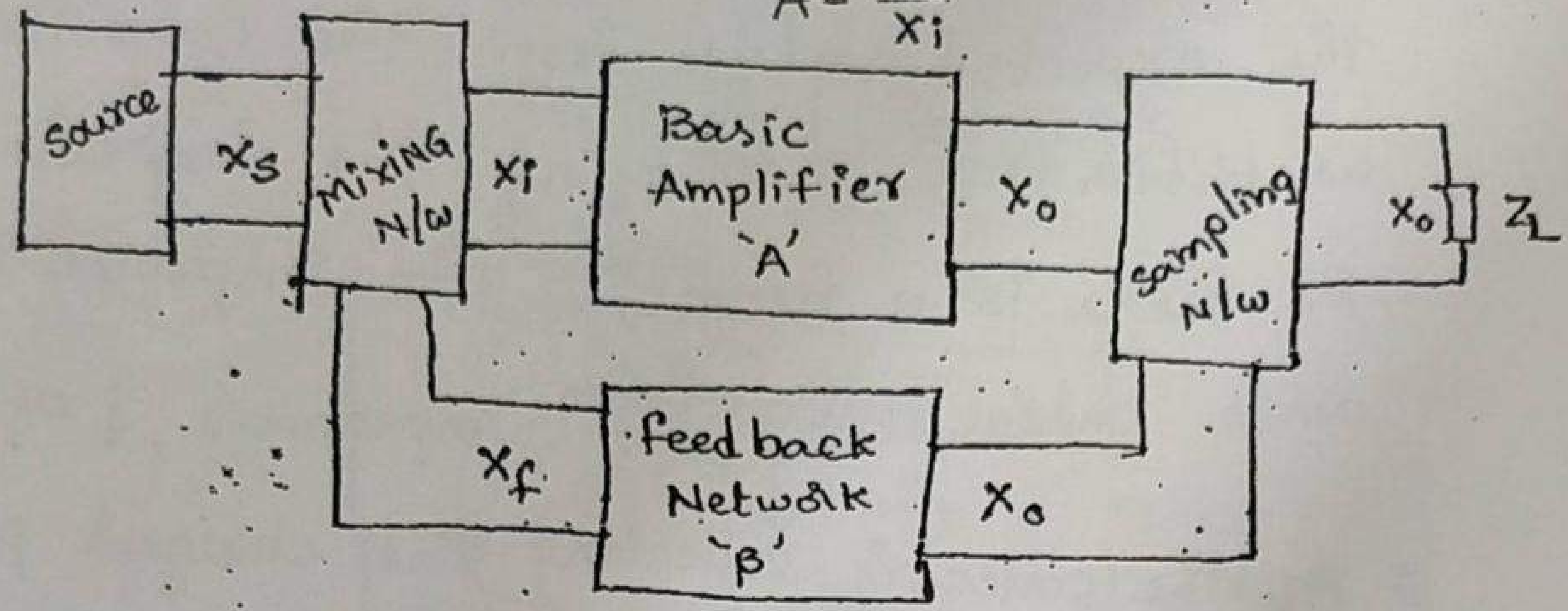
But as temp↑, A_v↑ for CE amplifier i.e this CE amplifier suffers from stability problem. There is a necessity to increase the thermal stability

To ↑ thermal stability & To improve the impedan characteristics negative feedback employed.

Negative Feedback Amplifiers:-

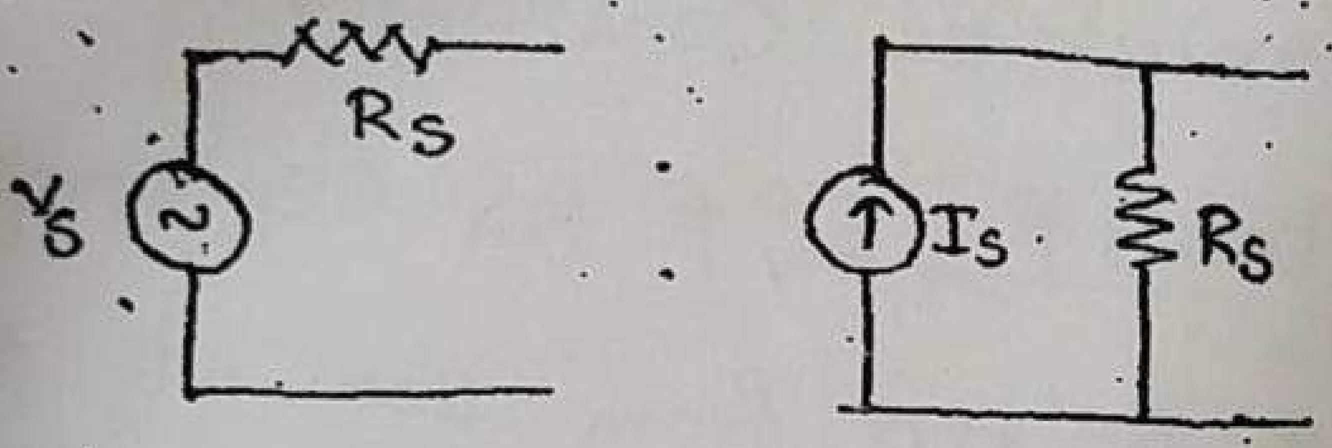
Block diagram:-

$$A = \frac{X_o}{X_i}$$



$$\beta = \left(\frac{X_f}{X_o}\right)$$

1. **Source:-**



2. **Mixing N/ω:-**

This N/ω combines the signals coming from source & feedback N/ω.

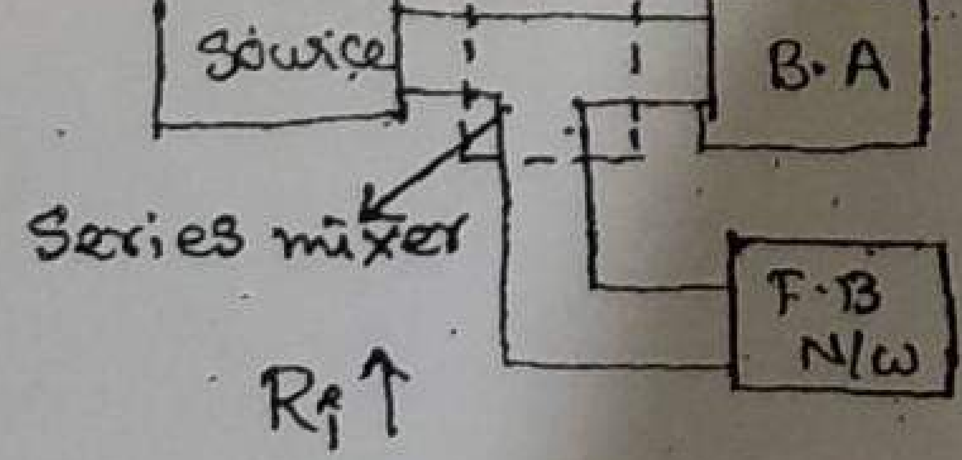
* In Neg feed back Amp. the mixer is a differential N/ω.

$$\boxed{X_i = X_s - X_f}$$

* Depending on mixing of signals, the mixing n/w's are classified into

1. **Series mixer:-**

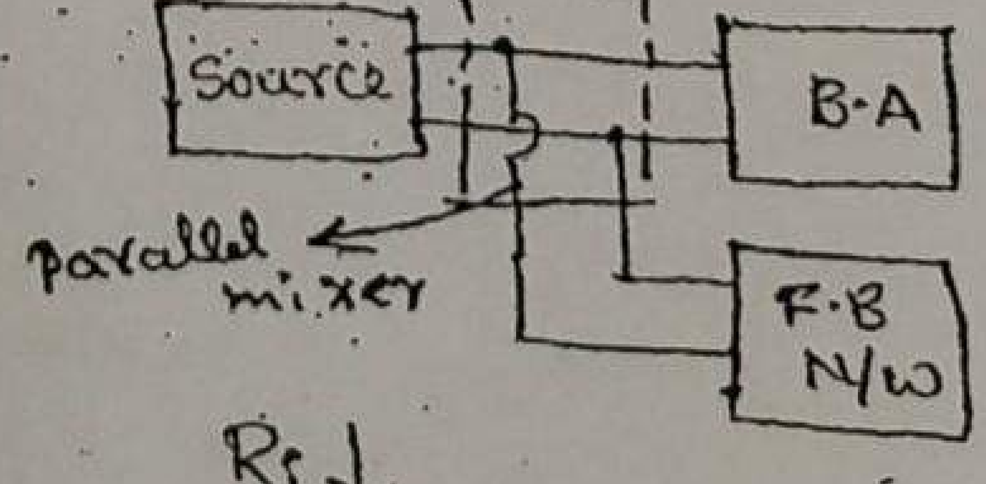
we mix the voltage signals in series



$R_i \uparrow$

2. **Shunt mixer:-**

we mix current signals in parallel



$R_i \downarrow$

3. Basic Amplifier:-

Depending on the i/p & o/ps of the Basic amp, they classified into:

1. Voltage amplifier, $A_V = \left(\frac{V_o}{V_i}\right)$

2. Current Amplifier, $A_I = \left(\frac{I_o}{I_i}\right)$

3. Trans resistance Amplifier, $R_m = \left(\frac{V_o}{I_i}\right)$

4. Trans conductance Amplifier, $G_m = \left(\frac{I_o}{V_i}\right)$

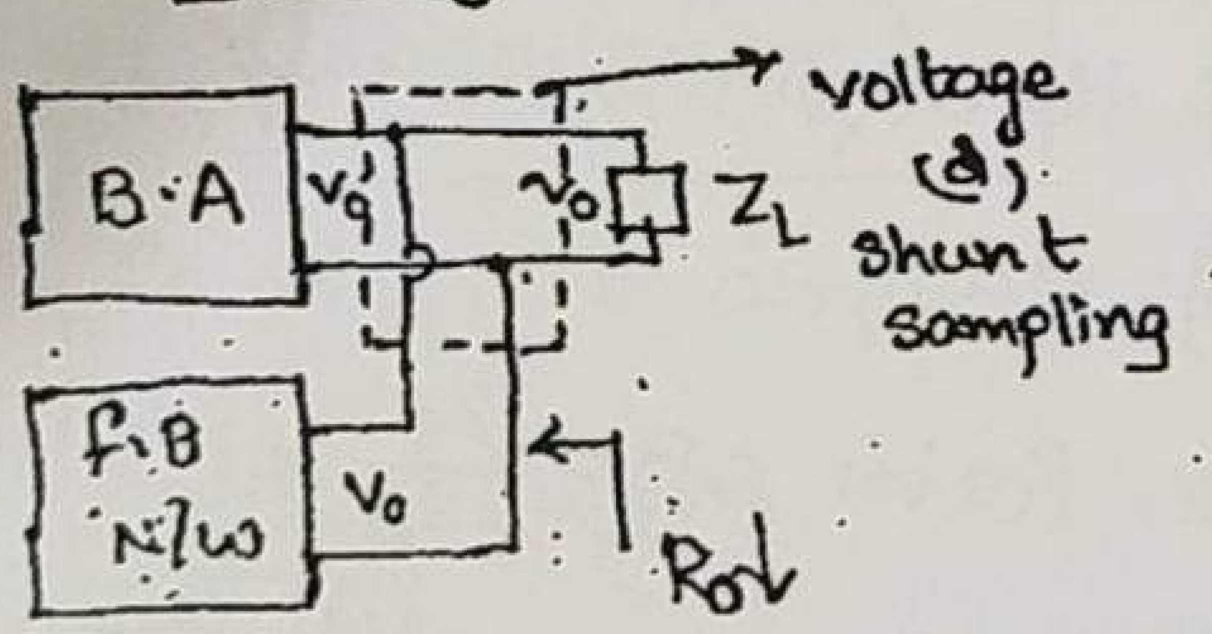
4. Sampling N/w:-

This n/w connects the o/p of Basic amplifier as i/p to the feedback N/w

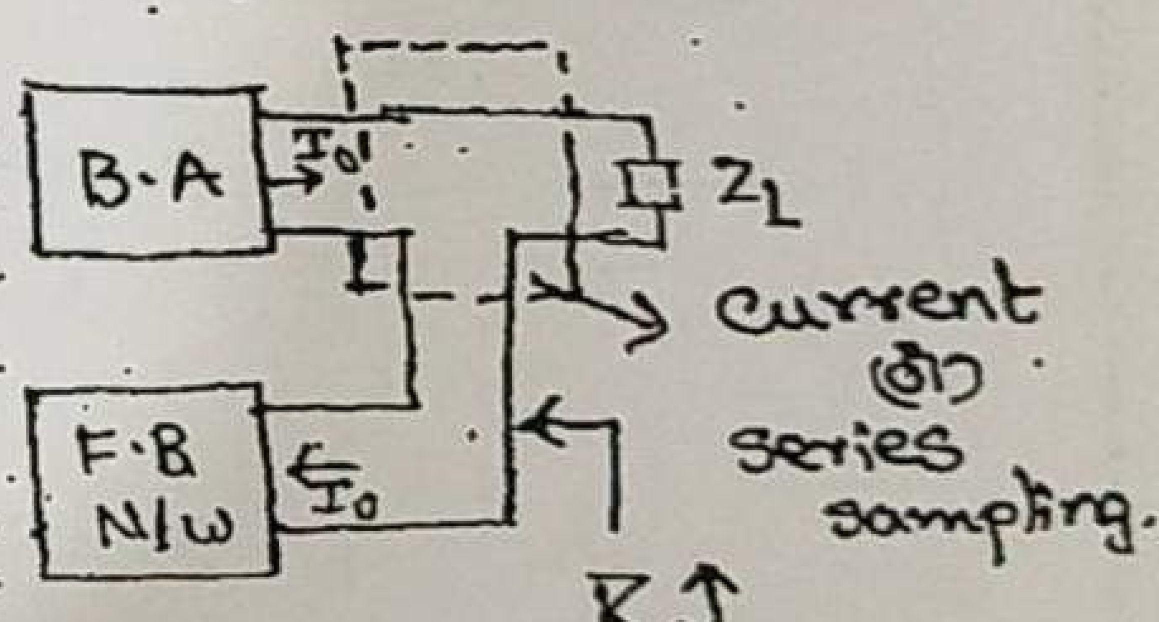
- Depending on the o/p of Basic Amp - the sampling N/w are classified into

① voltage sampling ② current sampling.

1- voltage sampling:



2. current sampling:-



5. Feedback N/w:- A part of the B·A o/p is given as i/p to the Basic Amplifier through feedback N/w. This n/w reduces the signal strength. This n/w also called Attenuator N/w.

- This n/w consists only Resistors.

$$\beta = \frac{X_f}{X_o}, \quad X_f < X_o \Rightarrow \beta < 1 \Rightarrow \boxed{0 < \beta < 1}$$

where

$\beta \rightarrow$ Feedback factor (or) Ratio Attenuation factor (or)

Retransmission factor (or) Ratio.

* Depending on <u>sampling N/w</u> & <u>Mixing N/w</u>, the NFB Amplifier are classified into :

1. Voltage - series (OR) shunt - series NFB Amp.

Most preferably. ✓ $R_o \downarrow$ $R_i \uparrow$ ✓

2. Voltage - shunt (OR) shunt - shunt NFB Amp.

✓ $R_o \downarrow$ $R_i \downarrow$ ×

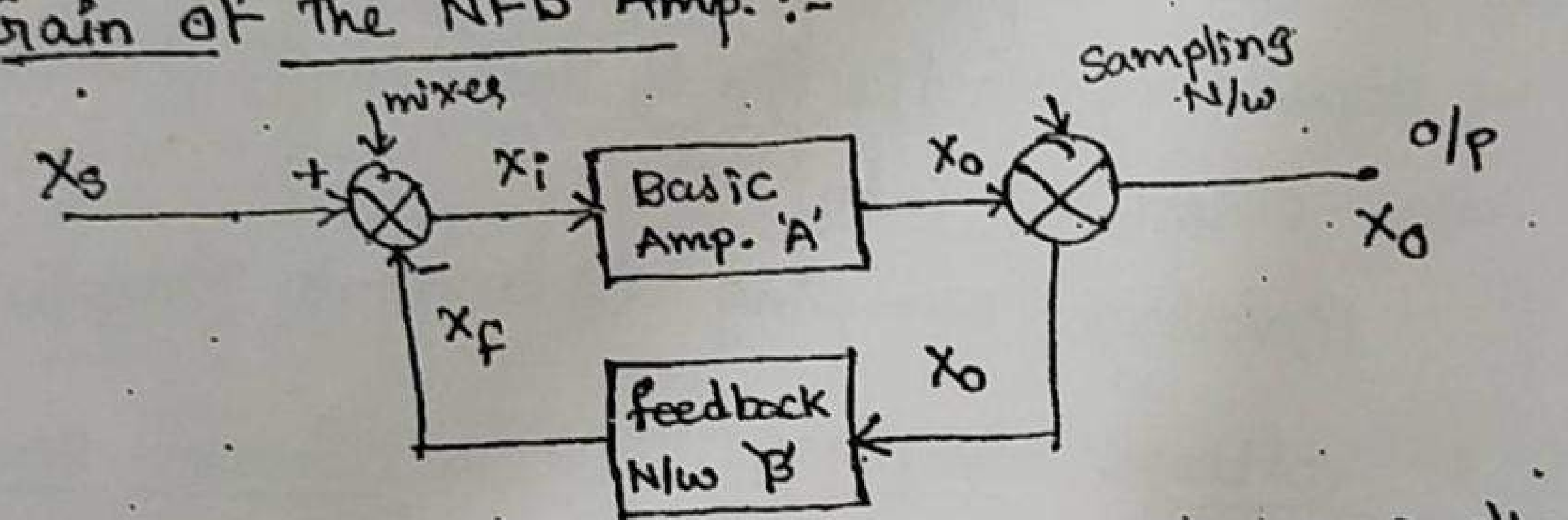
3. current - series (OR) series - series NFB Amp.

× $R_o \uparrow$ $R_i \uparrow$ ✓

4. current - shunt (OR) series - shunt NFB Amp.

least. × $R_o \uparrow$ $R_i \downarrow$ ×

<u>Gain of the NFB Amp.</u> :-



A → Gain of the amplifier without feedback

$$A = \left(\frac{X_o}{X_i}\right)$$

β → feedback factor, $\beta = \frac{X_f}{X_o}$, $\beta < 1$

A_f → Gain of the amp. with feed back

$$A_f = \frac{X_o}{X_s}$$

$X_o = AX_i$

with feed back $X_i = X_s - X_f$

$$X_o = A(X_s - X_f)$$
$$= AX_s - AX_f$$
$$= AX_s - A(\beta X_o)$$

$$X_o(1+\beta A) = AX_s$$

$$\boxed{\frac{X_o}{X_s} = A_f = \frac{A}{1+\beta A}}$$

for NFB Amp, $(1+\beta A)>1$

$$\boxed{A_f < A}$$

* The gain with feedback reduced by a factor of $(1+\beta A)$.
* The reduced gain → ↑ the Stability.
  → ↑ the Band width.
  → ↓ the Noise.
  → ↓ the distortion.

* The general char. of NFB Amplifiers :-

1. stability more
2. Increased Bandwidth
3. Decreased Noise
4. Decreased Distortion
5. i/p & o/p resistances changes appreciably depends on type of feedback.

1. stability More :-

$$\boxed{A_f = \left(\frac{A}{1+\beta A}\right)}$$

for Neg F.B amplifier, $(1+\beta A)>1$.

Case(i): $(1+\beta A) \rightarrow$ very high

$1+\beta A \simeq \beta A$

$$A_f \simeq \frac{\cancel{A}}{\beta \cancel{A}}$$

$$\boxed{A_f \simeq \frac{1}{\beta}}$$

A_f depends only β - 'β' is constant. A_f is also constant. As A_f is independent of 'A' → The N.F.B Amp thermally More stable.

Case (ii) :-

$$A_f = \frac{A}{1+\beta A}$$

Diff w.r.t A

$$\frac{dA_f}{dA} = \frac{(1+\beta A)(1) - A(\beta)}{(1+\beta A)^2}$$

$$= \frac{1}{(1+\beta A)^2}$$

$$\frac{dA_f}{dA} = \frac{1}{(1+\beta A)} \left(\frac{1}{(1+\beta A)} \frac{A}{A}\right)$$

$$\frac{dA_f}{dA} = \frac{1}{(1+\beta A)} \frac{A_f}{A}.$$

$$* \boxed{\frac{dA_f}{A_f} = \frac{1}{1+\beta A} \frac{dA}{A}}$$

$\frac{dA_f}{A_f} \rightarrow$ % change in gain with feedback.

$\frac{dA}{A} \rightarrow$ " " without " .

$$\frac{\left(\frac{dA_f}{A_f}\right)}{\left(\frac{dA}{A}\right)} = \frac{\text{sensitivity } (S) = \left(\frac{1}{1+\beta A}\right)}{\text{As } (1+\beta A) > 1, (S<1)}$$

$$\boxed{\left(\frac{dA_f}{A_f}\right) < \left(\frac{dA}{A}\right)}$$

→ This shows that the NFB Amp. is thermally stable comp. with F.B. ~~amy~~ amplifier.

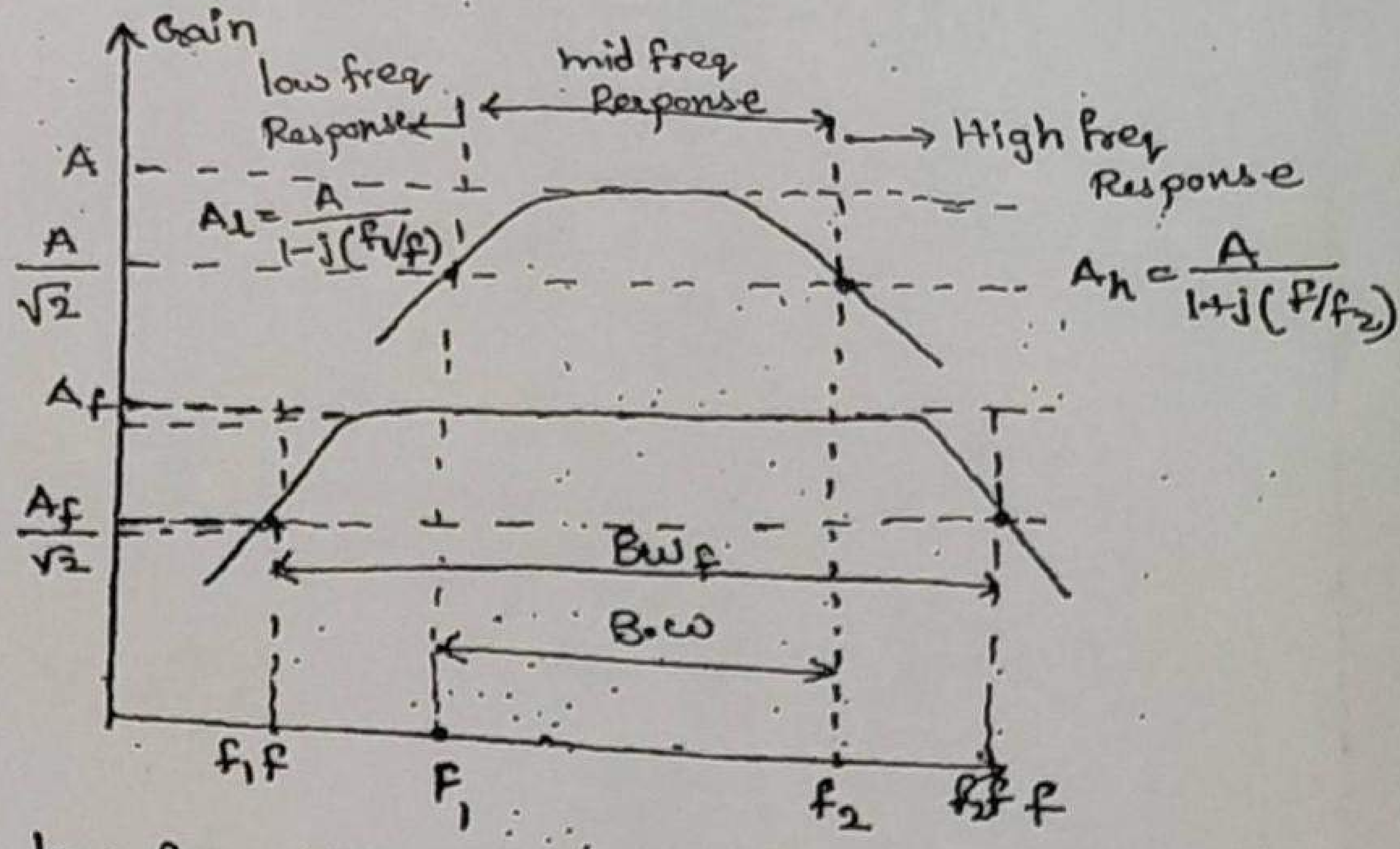
$$D = \frac{1}{S} = (1+\beta A) \Rightarrow \underline{D > 1}.$$

2. Band with increases :-

* The gain bandwidth product of any system with & without feedback is CONSTANT.

$$A_f \, BW_f = A \times BW$$

$$\frac{\cancel{A}}{1+\beta A} BW_f = \cancel{A} \times BW \Rightarrow \boxed{BW_f = BW(1+\beta A)}$$



From the low freq response of the Amp.

$$A_l = \frac{A}{1-j(f_1/f)}$$

$$A_{lf} = \frac{A_l}{1+\beta A_l} = \frac{\frac{A}{1-j(f_1/f)}}{1+\beta\left(\frac{A}{1-j(f_1/f)}\right)}$$

$$A_{lf} = \frac{\frac{A}{\cancel{1-j(f_1/f)}}}{\frac{1-j(f_1/f)+\beta A}{\cancel{1-j(f_1/f)}}} = \frac{A}{(1+\beta A)-j(f_1/f)}$$

$$= \frac{A}{(1+\beta A)\left[1-j\left(\frac{f_1}{f(1+\beta A)}\right)\right]}$$

$$= \frac{A/(1+\beta A)}{1-j\left(\frac{f_1/(1+\beta A)}{f}\right)}$$

$$\boxed{A_{lf} = \frac{A_f}{1-j\left(\frac{f_1 f}{f}\right)}}$$

$f_1 f = \frac{f_1}{1+\beta A}$, As $(1+\beta A) > 1$; $f_1 f < f$.

∴ The lower cut off freq reduced by a factor of $(1+\beta A$

lly from high freq response of the Amplifier,

$$\boxed{f_{2f} = f_2 (1+\beta A)}$$

The upper cutoff freq with feedback increased by a factor of $(1+\beta A)$.

3. Noise Decreases:-

As BW↑ Noise↓

Let N → Noise of amp without feedback.

N_f → " " with "

$$\boxed{N_f = \frac{N}{1+\beta A}}$$

4. Distortion Decreases:-

As BW↑ Distortion↓

Let D → Distortion of the amp without f/B.

D_f → " " " with ".

$$\boxed{D_f = \frac{D}{1+\beta A}}$$

5. i/p & o/p resistances changes appreciably:-

Let R_i → i/p Resistance of the amp without feedback.

R_o → o/p " " " without ".

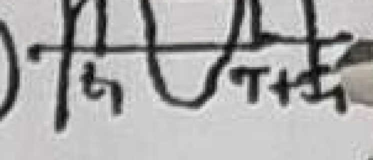
R_{if} → i/p " " " with ".

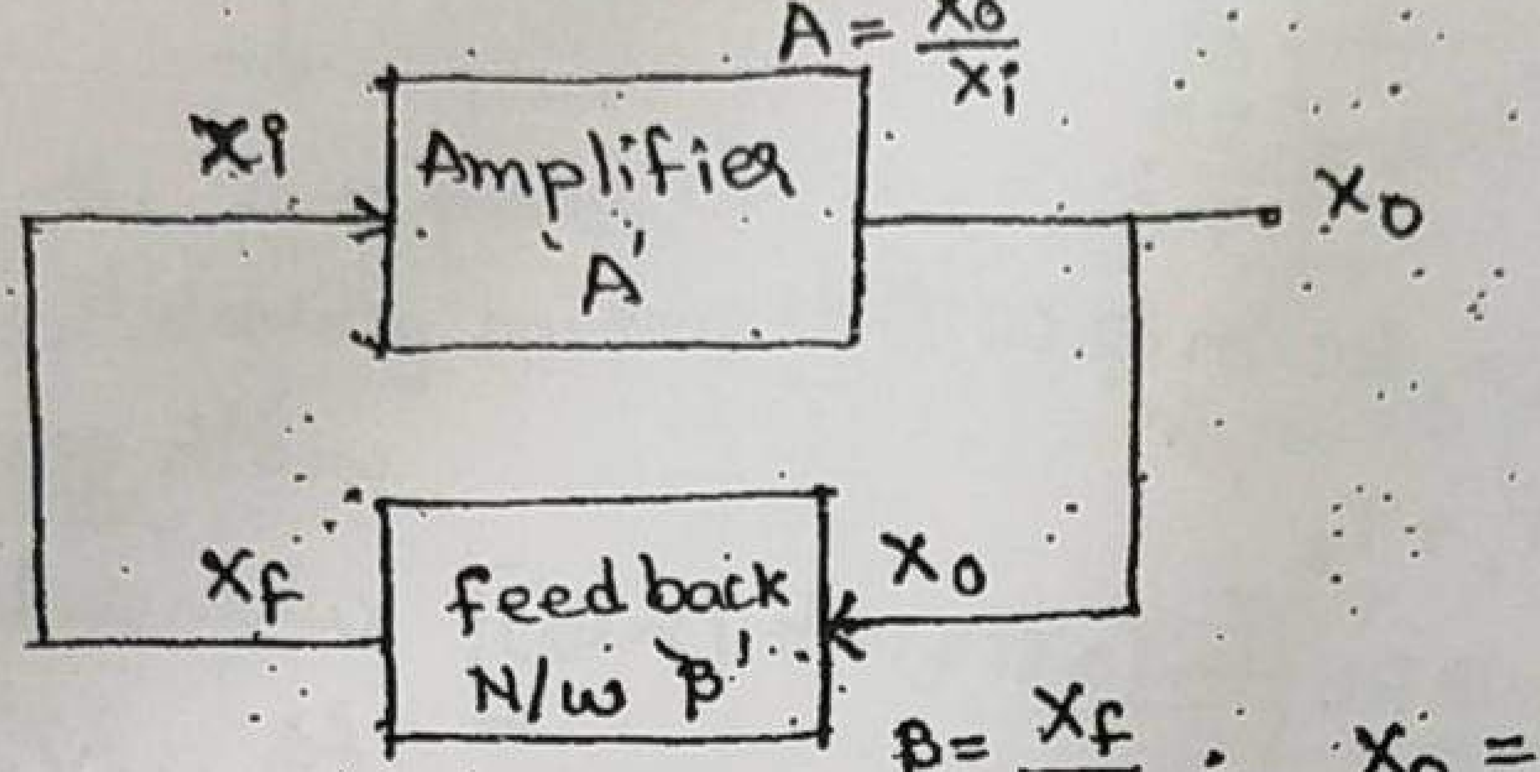
R_{of} → o/p " " " " ".

N.F.B amp	o/p Resistance	i/p Resistance
Voltage - series	$R_{of} = \frac{R_o}{1+\beta A}$ ↓	$R_{if} = R_i(1+\beta A)$ ↑
Voltage - shunt	$R_{of} = \frac{R_o}{1+\beta A}$ ↓	$R_{if} = \frac{R_i}{(1+\beta A)}$ ↓
Current - series	$R_{of} = R_o(1+\beta A)$ ↑	$R_{if} = R_i(1+\beta A)$ ↑
Current - shunt	$R_{of} = R_o(1+\beta A)$ ↑	$R_{if} = \frac{R_i}{(1+\beta A)}$ ↓.

Sinusoidal oscillators:-

A ckt which generates undamped sinusoidal oscillations is called sinusoidal (or) Harmonic oscillator.

*(undamped means Amplitude constant "periodically") 



$\beta = \frac{X_f}{X_o}$; $X_o = \frac{X_f}{\beta}$

In oscillators, $X_f = X_i$

$$X_o = AX_i$$

$$\frac{X_f}{\beta} = AX_i \Rightarrow \boxed{X_f = A\beta X_i}$$

$$\therefore A\beta = 1$$

$A\beta \rightarrow$ loop gain

$$A\beta = 1 = 1 + j0 = 1\angle 0^\circ.$$

(i) The magnitude of loop gain = 1.
(ii) The total phase of the loop is 0° (or) 360°

} "BARKHAUSEN" CRITERIA : Conditions.

To get undamped oscillations the ckt must satisfy the above conditions.

→ If the amplifier introduces 180° of phase [Inverting amplifier, CE amplifier] the remaining 180° must introduced by the feedback.

→ If the amplifier introduces 0° of phase [Non-inverting Amplifier, CE-CE cascaded Amplifier] the feedback N/w must introduce 0° of phase.

→ The Feed back N/ω consists $\underline{R, L, C}$ → in oscillators
The transfer function of the feed back N/ω.

$$\Rightarrow \frac{X_f(s)}{X_o(s)} = \beta = \beta_{real} \pm j\,\beta_{imagnary}.$$

The gain of the amplifier 'A' → is alway real valu

The magnitude of the loop gain, $\boxed{A\beta = 1}$

$\therefore \beta = \frac{1}{A}$ → must be rea

→ To get undamped oscillation, the imaginary part of 'β' must be zero.

$$\Rightarrow \boxed{\beta_{imaginary} = 0}$$

from this we get the freq of oscillations generated by the ckt.

→ The feed back factor $\boxed{\beta = \beta_{real}}$.

The gain of the amplifier $A = \frac{1}{\beta}$

$$\Rightarrow \boxed{A = \frac{1}{\beta_{real}}}$$

→ Depending on the components used in the feed back N/ω, the oscillators are classified into:

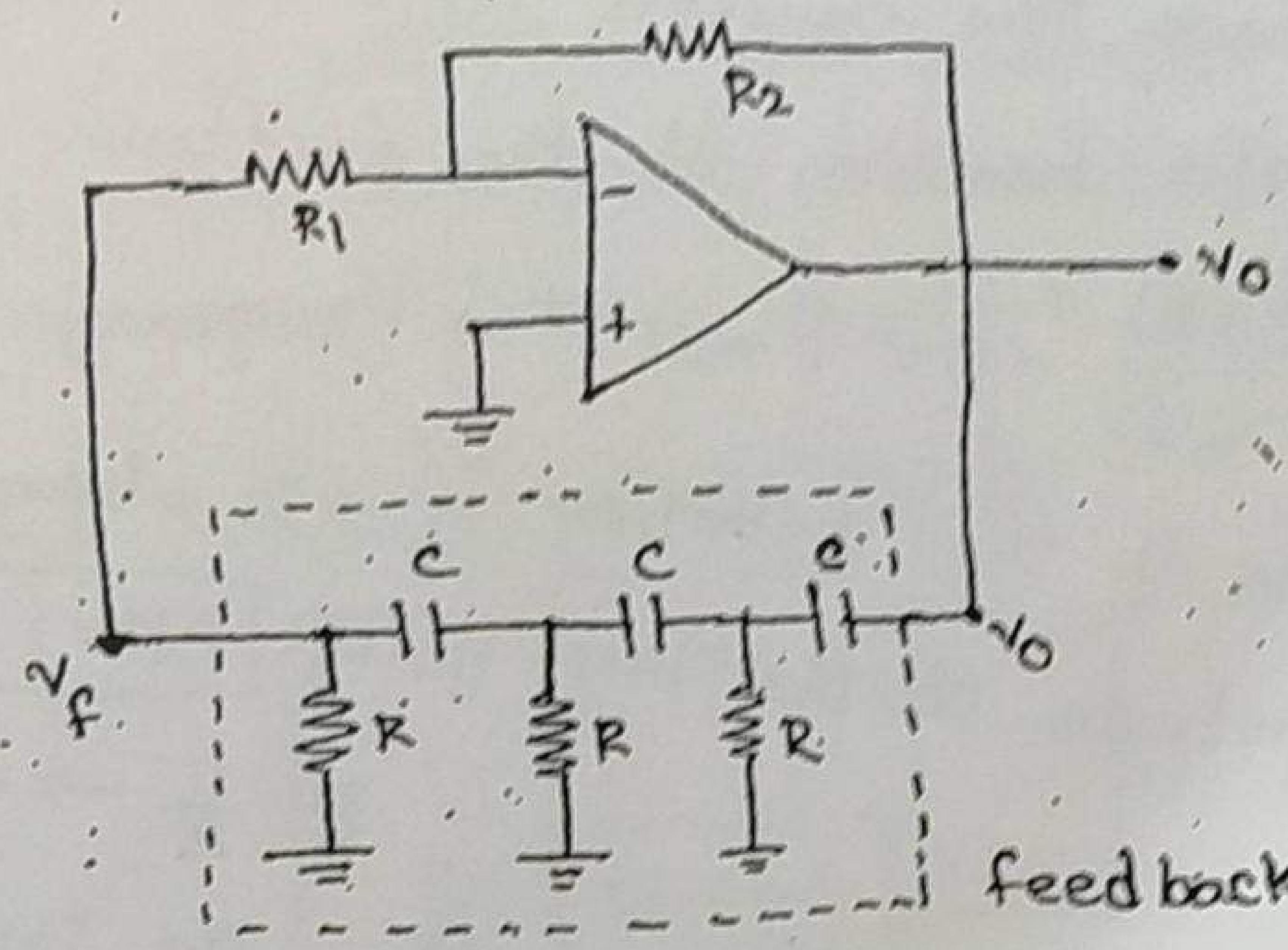
1. RC oscillators
   - RC phase shift oscillator
   - wein Bridge oscillator

   } Audio frequency oscillators.

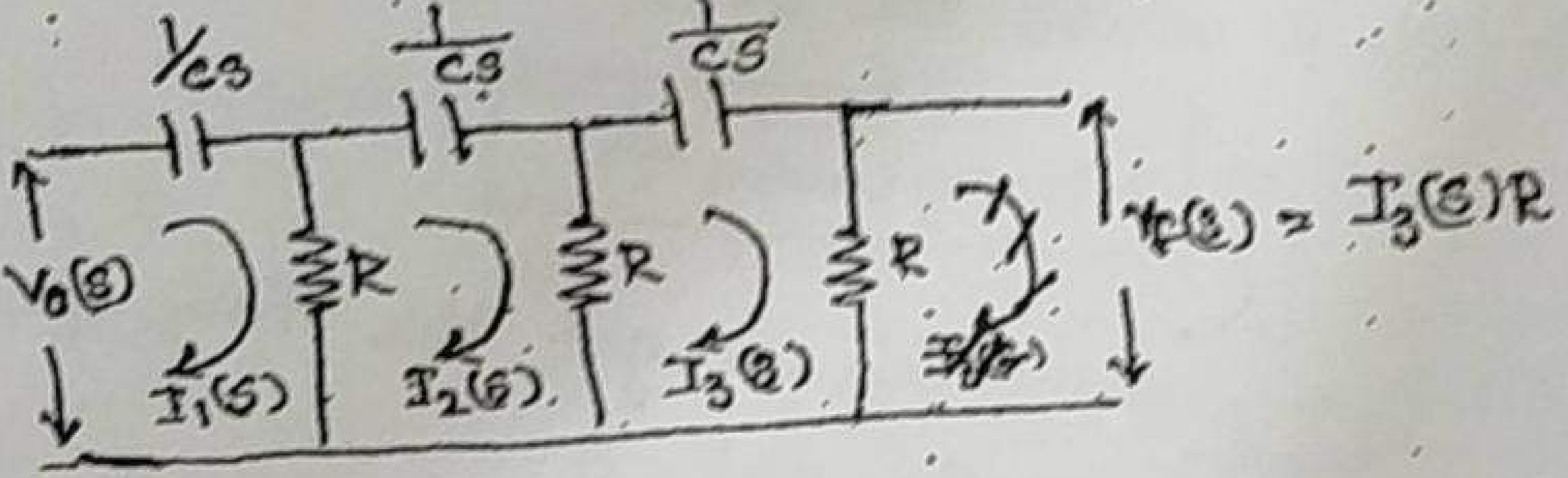
2. LC oscillators
   - Hartely oscillator
   - colpitt's oscillator

   } Radio freq oscillators.

1. RC phase shift oscillator:



<u>Find the transfer function:-</u>



$$V_o(s) = I_1(s)\left[R+\frac{1}{sC}\right] - I_2(s)R \longrightarrow (1)$$

$$0 = -I_1(s)R + I_2(s)\left[2R+\frac{1}{sC}\right] - I_3(s)R \longrightarrow (2)$$

$$0 = -I_2(R) + I_3(s)\left[2R+\frac{1}{sC}\right] \longrightarrow (3)$$

$$\begin{bmatrix} R+\frac{1}{sC} & -R & 0 \\ -R & 2R+\frac{1}{sC} & -R \\ 0 & -R & 2R+\frac{1}{sC} \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \\ I_3(s) \end{bmatrix} = \begin{bmatrix} V_o(s) \\ 0 \\ 0 \end{bmatrix}$$

$$A = R+\frac{1}{sC}\left[\left(2R+\frac{1}{sC}\right)^2 - R^2\right] + R\left[-R\left[2R+\frac{1}{sC}\right]\right]$$

$$= \left(R+\frac{1}{sC}\right)\left[3R^2+\frac{1}{s^2C^2}+\frac{4R}{sC}\right] - R^2\left(2R+\frac{1}{sC}\right)$$

$$= 3R^3 + \frac{R}{s^2C^2} + \frac{4R^2}{sC} + \frac{3R^2}{sC} + \frac{1}{s^3C^3} + \frac{4R}{s^2C^2} - 2R^3 - \frac{R^2}{sC}$$

$$\Delta = R^3 + \frac{6R^2}{sC} + \frac{5R}{s^2C^2} + \frac{1}{s^3C^3}.$$

$$\Delta_3 = \begin{bmatrix} R+\frac{1}{sC} & -R & V_0(s) \\ -R & 2R+\frac{1}{sC} & 0 \\ 0 & -R & 0 \end{bmatrix} = V_0(s)\left[R^2 - 0\right]$$

$$= V_0(s) R^2$$

$$I_3(s) = \frac{\Delta_3}{\Delta} = \frac{V_0(s) R^2}{R^3 + \frac{6R^2}{sC} + \frac{5R}{s^2C^2} + \frac{1}{s^3C^3}}$$

$$V_f(s) = I_3(s) R = \frac{V_0(s)\, R^3}{R^3 + \frac{6R^2}{sC} + \frac{5R}{s^2C^2} + \frac{1}{s^3C^3}}$$

$$V_f(s) = \frac{V_0(s)}{1 + \frac{6\cancel{R^2}}{sC\cancel{R^3}} + \frac{5\cancel{R}}{s^2C^2\cancel{R^3}2} + \frac{1}{s^3C^3R^3}}$$

$$V_f(s) = \frac{V_0(s)}{1 + \frac{6}{sCR} + \frac{5}{s^2C^2R^2} + \frac{1}{s^3C^3R^3}}$$

$$T.F = \frac{V_f(s)}{V_0(s)} = \frac{1}{1 + \frac{6}{sCR} + \frac{5}{s^2C^2R^2} + \frac{1}{s^3C^3R^3}}$$

put $s = j\omega$.

$$T.F = \beta = \frac{1}{1 - j\frac{6}{\omega CR} + (-1)\frac{5}{\omega^2C^2R^2} + j\frac{1}{\omega^3C^3R^3}}$$

$$= \frac{1}{\left(1 - \frac{5}{\omega^2C^2R^2}\right) + j\left(\frac{1}{\omega^3C^3R^3} - \frac{6}{\omega CR}\right)}$$

To get undamped oscillations, the imaginary part of β must be zero.

$$\frac{1}{\omega^3 C^3 R^3} = \frac{6}{\omega C R}$$

$$\omega^2 C^2 R^2 = \frac{1}{6} \Rightarrow \omega^2 = \frac{1}{R^2 C^2 (6)} \Rightarrow \omega = \frac{1}{RC\sqrt{6}}$$

$$2\pi f = \frac{1}{RC\sqrt{6}}$$

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}}$$

The feedback factor is

$$\beta = \frac{1}{1 - \frac{5}{\omega^2 C^2 R^2}} = \frac{1}{1 - 5(6)}$$

$$\boxed{\beta = \frac{-1}{29}}$$

180° of phase b/w V_o & V_f.

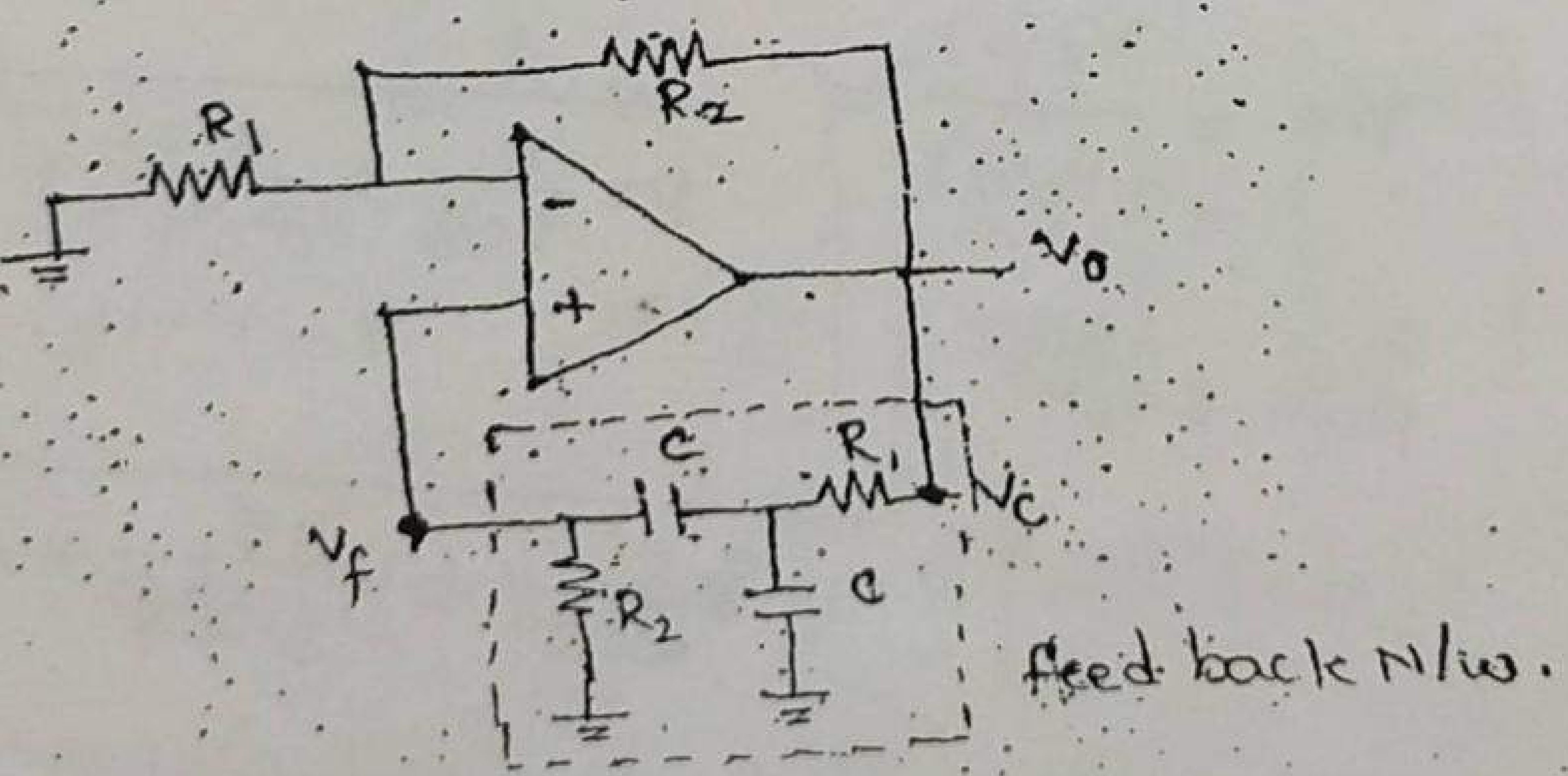
The gain of the amplifier $A = \frac{1}{\beta} = -29$.

$\therefore \boxed{A = -29}$

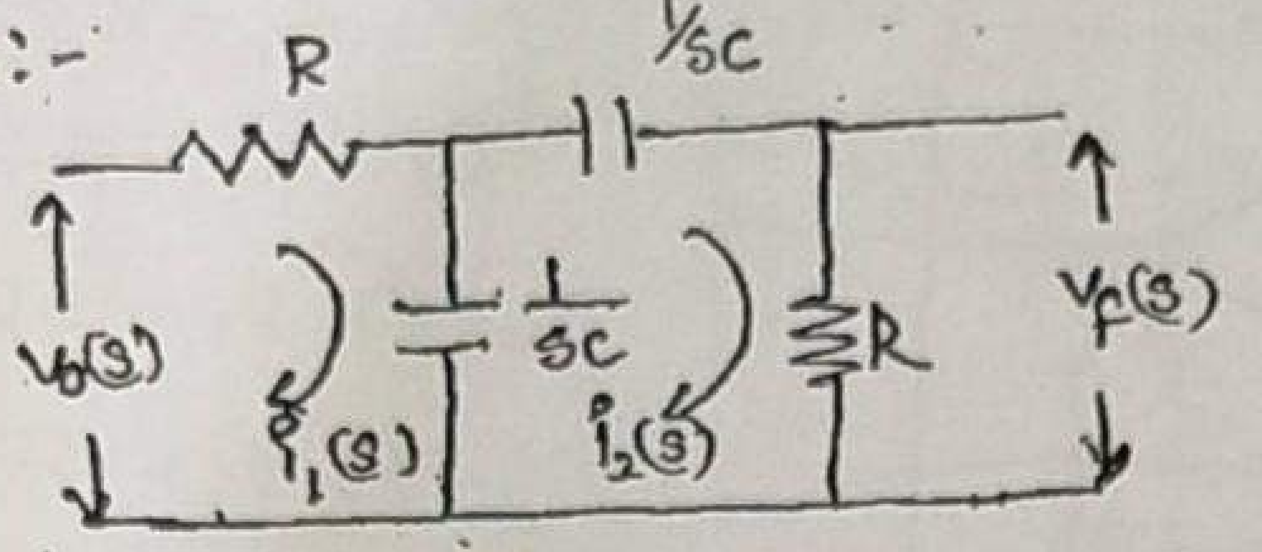
$$A = \frac{+R_2}{R_1} = +29$$

$\boxed{R_2 = 29R_1}$ $\therefore$ Each RC N/w introduces $\underline{60°}$ of phase in the above ckt.

1. calculate the freq of oscillations generated by the op-amp ckt shown & also calculate the Relation ship b/w R_1 & R_2.



Sol :-



$$V_0(s) = I_1(s)\left[R + \frac{1}{sC}\right] - I_2(s)\frac{1}{sC} \longrightarrow (1)$$

$$0 = I_2(s)\left[\frac{2}{sC} + R\right] - I_1(s)\frac{1}{sC} \longrightarrow (2)$$

from eq (2)

$$\frac{I_1(s)}{sC} = I_2(s)\left[R + \frac{2}{sC}\right]$$

substitute $I_1(s)$ in eq (1)

$$I_1(s) = I_2(s)\left[sCR + 2\right]$$

$$V_0(s) = I_2(s)\left[sCR + 2\right]\left[R + \frac{1}{sC}\right] - I_2(s)\frac{1}{sC}$$

$$= I_2(s)\left[sCR^2 + R + 2R + \frac{2}{sC} - \frac{1}{sC}\right]$$

$$= I_2(s)\left[sCR^2 + 3R + \frac{1}{sC}\right]$$

$$V_0(s) = \frac{I_2(s)}{sC}\left[s^2C^2R^2 + 3sCR + 1\right]$$

But $V_f(s) = I_2(s)R$

$$I_2(s) = \frac{V_f(s)}{R}$$

$$V_0(s) = \frac{V_f(s)}{sCR}\left[1 + 3sCR + s^2C^2R^2\right]$$

$$\frac{V_f(s)}{V_0(s)} = \left[\frac{sCR}{1 + 3sCR + s^2C^2R^2}\right]$$

$$T.F = \left[\frac{1}{3 + sCR + \frac{1}{sCR}}\right]$$

put $s = j\omega$

$$\beta = \frac{1}{3 + j\omega CR - j\frac{1}{\omega CR}}$$

$$= \frac{1}{3 + j\left[\omega CR - \frac{1}{\omega CR}\right]}$$

To get undamped oscillation the imaginary part of 'β' must be zero.

$$\omega CR = \frac{1}{\omega CR}$$

$$\omega = \frac{1}{RC}$$

$$\boxed{f = \frac{1}{2\pi RC}}$$

feedback factor $\beta = \frac{1}{3}$

Gain of the Amp $A = \frac{1}{\beta}$

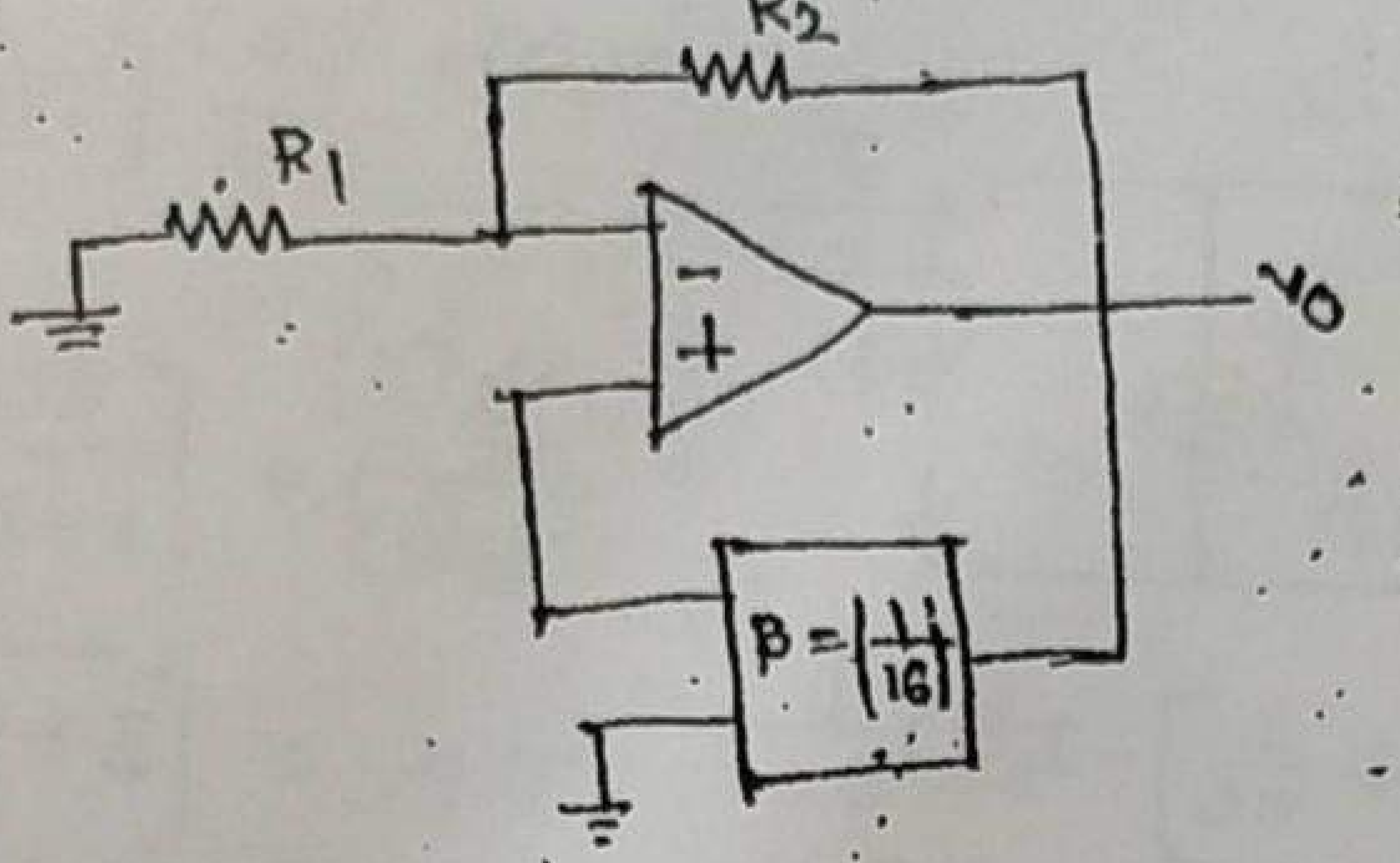
$$\boxed{A = 3}$$

$$A = 1 + \frac{R_2}{R_1} = 3$$

$$\frac{R_2}{R_1} = 2$$

$$\therefore \boxed{R_2 = 2R_1}$$

⇒



(a) $R_2 = 16 R_1$

(b) $R_1 = 16 R_2$

(c) $R_2 = 15 R_1$

(d) $R_1 = 15 R_2$

$f = 2KHz$

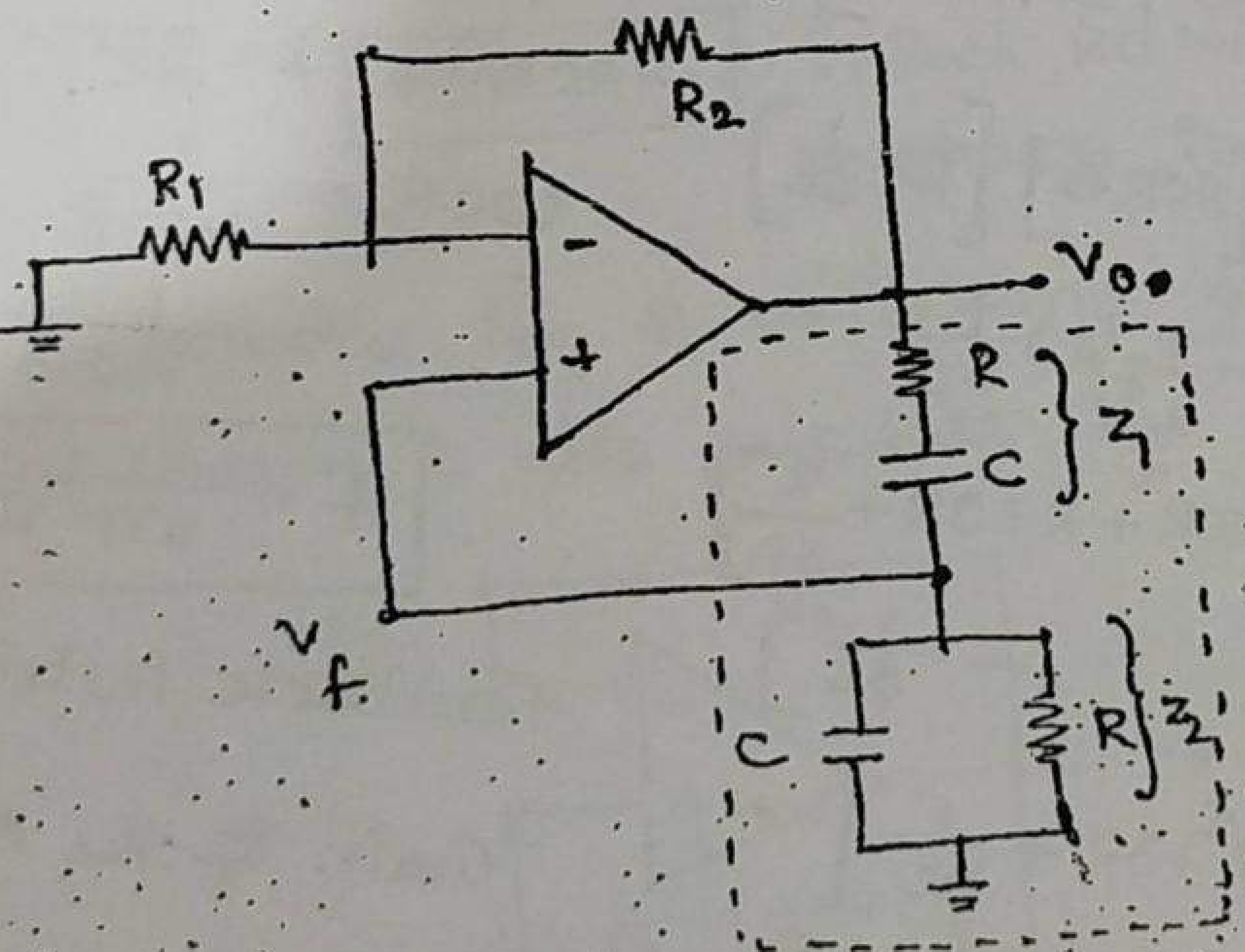
$$A\beta = 1$$

$$\therefore A = \frac{1}{\beta} = \frac{1}{\frac{1}{16}} = 16.$$

$$A = 1 + \frac{R_2}{R_1} = 16.$$

$$\Rightarrow \frac{R_2}{R_1} = 15 \Rightarrow \boxed{R_2 = 15 R_1}$$

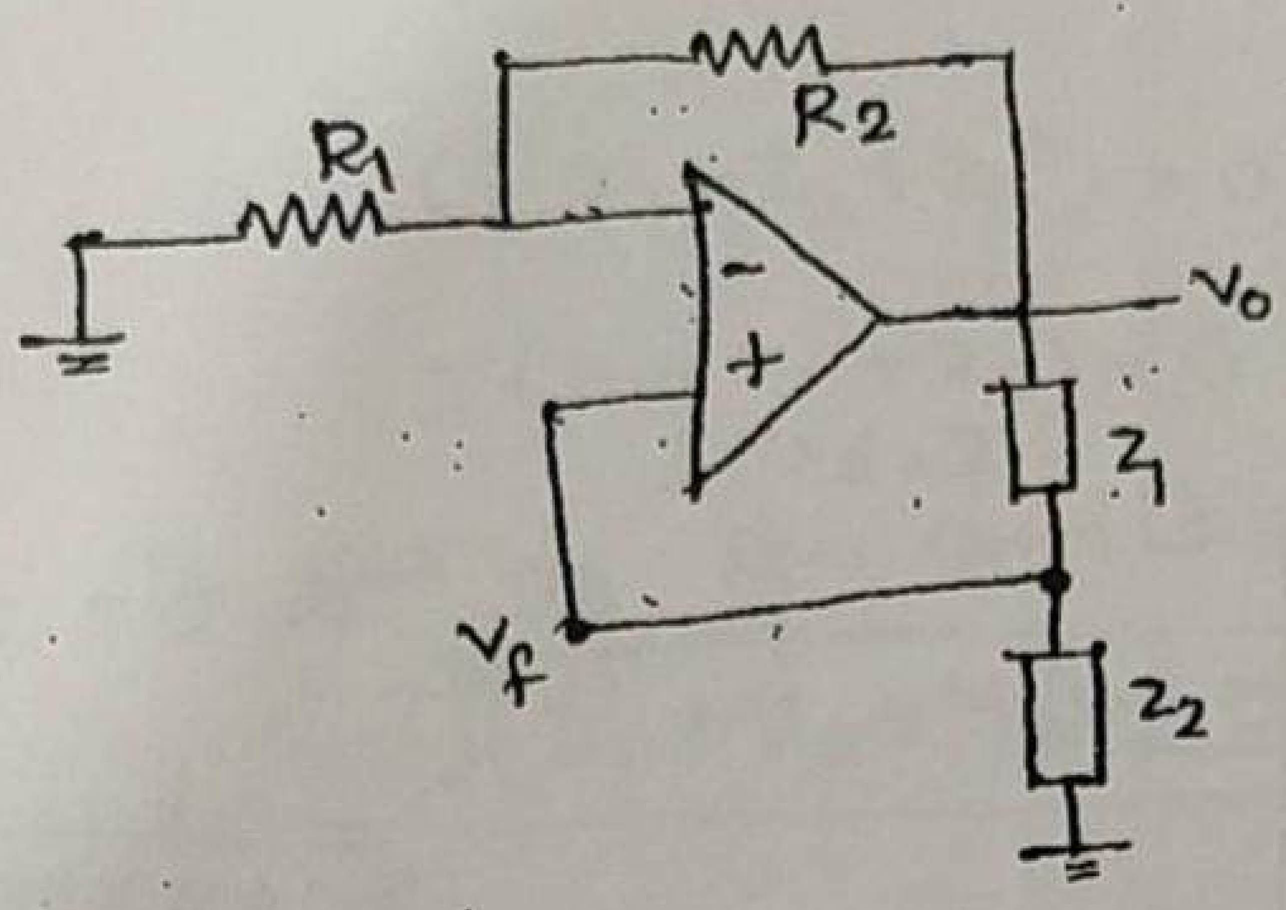
2. Wein Bridge oscillator:-



$$Z_1 = R + \frac{1}{cs} = \left(\frac{1+sCR}{sC}\right)$$

$$Z_2 = \frac{R \cdot \frac{1}{cs}}{R + \frac{1}{cs}} = \left(\frac{RCS}{sCR+1}\right)$$

Scanned by TapScanner



$$V_f(s) = V_o(s)\left[\frac{Z_2}{Z_1+Z_2}\right]$$

$$\frac{V_f(s)}{V_o(s)} = T.F = \beta = \left(\frac{Z_2}{Z_1+Z_2}\right)$$

$$\beta = \frac{\frac{R}{1+sCR}}{\frac{1+sCR}{sC} + \frac{R}{1+sCR}}$$

$$\beta = \frac{\frac{R}{\cancel{1+sCR}}}{\frac{(1+sCR)^2 + sCR}{\cancel{1+sCR}\,(sC)}} = \frac{sCR}{(1+sCR)^2+sCR}$$

$$= \frac{sCR}{1+s^2C^2R^2+2sCR+sCR}$$

$$= \frac{sCR}{1+s^2C^2R^2+3sCR}$$

$$\beta = \frac{1}{\frac{1}{sCR}+sCR+3}$$

* put $s = j\omega$

$$T.F = \beta = \frac{1}{-j\frac{1}{\omega CR} + j\omega CR + 3} = \frac{1}{3+j\left[\omega CR - \frac{1}{\omega CR}\right]}$$

To get undamped oscillations, the imaginary part 'β' must be zero.

$$\omega CR = \frac{1}{\omega CR}$$

$$\omega = \frac{1}{RC}$$

$$\boxed{f = \frac{1}{2\pi RC}}$$

feedback factor, $\beta = \frac{1}{3}$

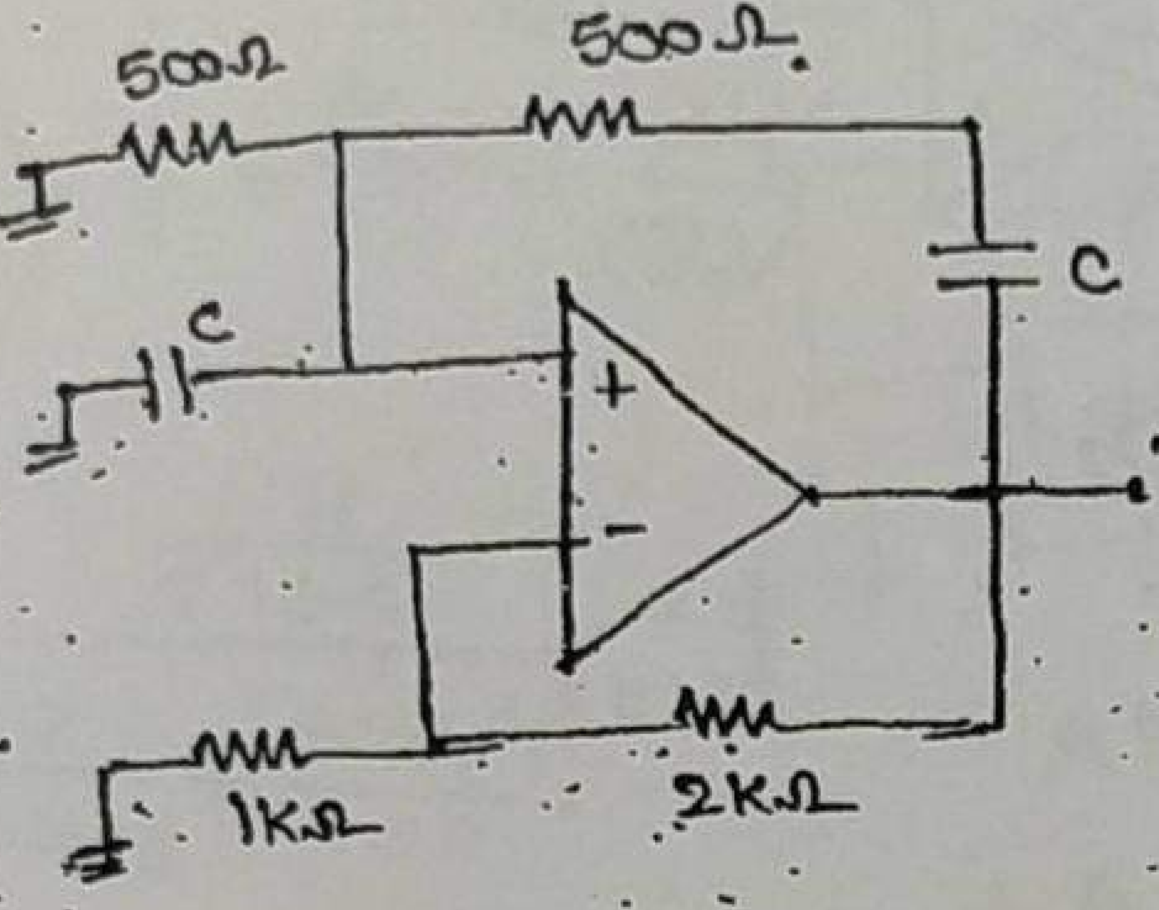
Gain of the Amp $A = \frac{1}{\beta}$

$$\boxed{A = 3}$$

$$A = 1 + \frac{R_2}{R_1} = 3$$

$$\frac{R_2}{R_1} = 2 \Rightarrow \boxed{R_2 = 2R_1}$$

pb:- The ckt shown



$\therefore f = 3\,KHz$

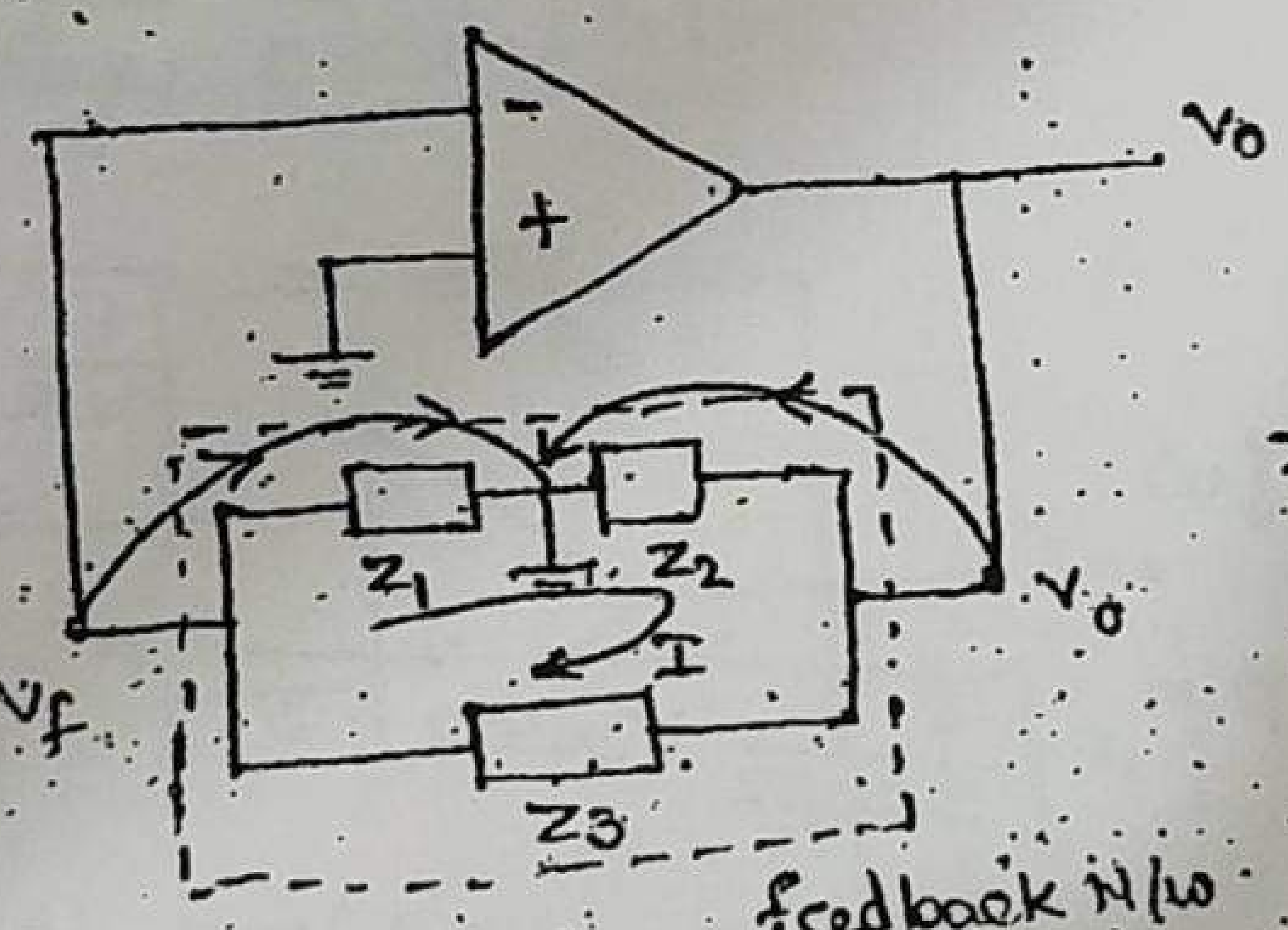
$f = \frac{1}{2\pi RC} \Rightarrow C = \frac{1}{2\pi f R}$

$= \frac{1}{2\pi \times 3 \times 10^3 \times 500} = \frac{1}{3\pi}\,\mu F$

LC oscillators :-

In LC oscillators, the feedback N/w consists Inductor & Capacitor only.

General form:-



Z_1 & Z_2 → same type elements (i.e L or C).

Z_3 → opposite type element (i.e C (or) L)

$v_f = I Z_1$

$\therefore v_o = -I Z_2$

The feed back factor, $\beta = \frac{v_f}{v_o} = \frac{I Z_1}{-I Z_2} \Rightarrow \boxed{\beta = \frac{-Z_1}{Z_2}}$.

The gain of the amp, $A = \frac{1}{\beta} = \frac{-Z_2}{Z_1} \Rightarrow \boxed{A = \frac{-Z_2}{Z_1}}$

for freq. of oscillations,

Apply KVL to feedback N/w.

$$0 - I(Z_1+Z_2+Z_3) = 0$$

$$I(Z_1+Z_2+Z_3) = 0$$

To satisfy this condition,

$$\boxed{(Z_1+Z_2+Z_3) = 0}$$

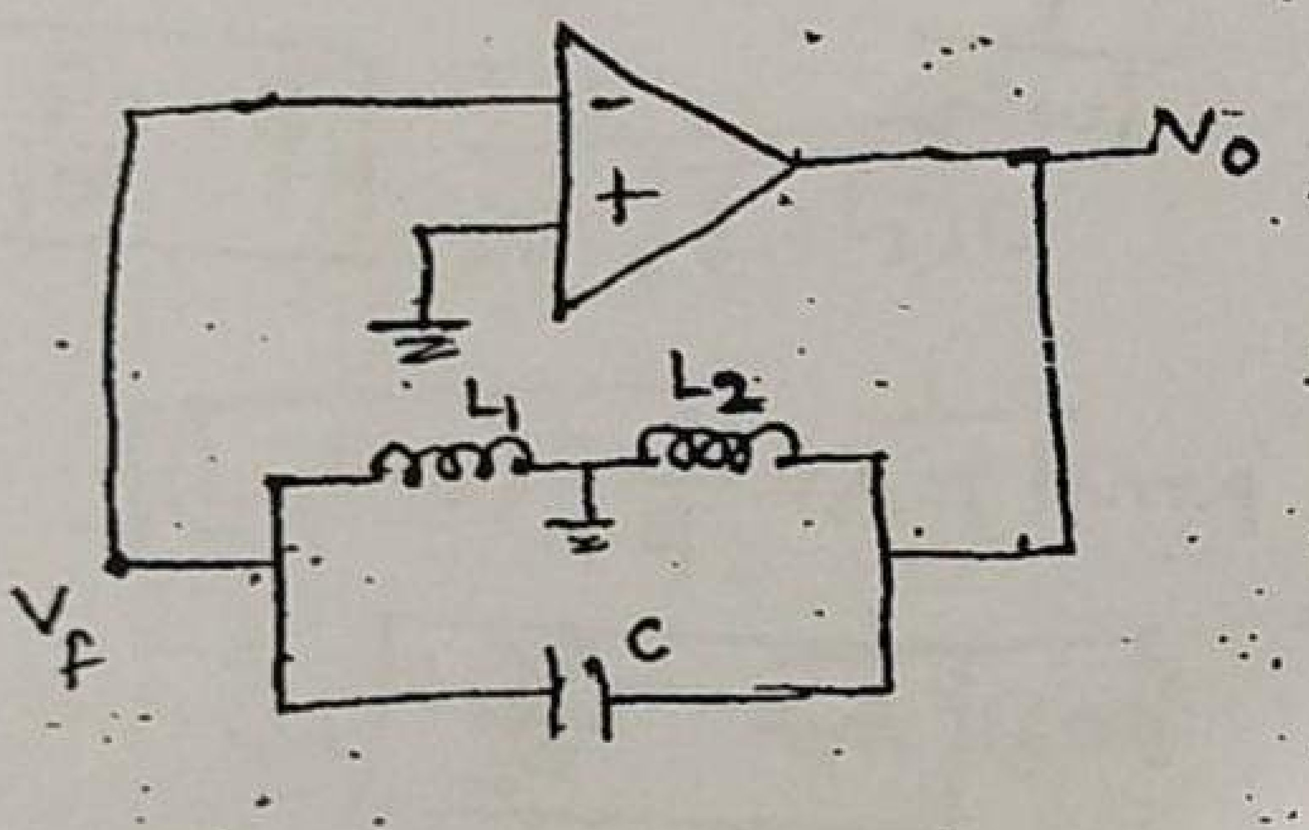
from this we get the freq of oscillations generated from the ckt.

1. **Hartely oscillator** :-

Z_1 & $Z_2 \rightarrow$ Inductors

$Z_3 \rightarrow$ capacitor

$$Z_1 = j\omega L_1 , \quad Z_2 = j\omega L_2 , \quad Z_3 = \frac{1}{j\omega C} = \frac{-j}{\omega C}$$



→ The feed back factor,

$$\beta = \frac{-Z_1}{Z_2} = \frac{-j\omega L_1}{j\omega L_2}$$

$$\boxed{\beta = \frac{-L_1}{L_2}} \qquad \boxed{L_2 > L_1}$$

$\therefore \beta < 1$.

→ The gain of the Amp. $A = \frac{1}{\beta} = \frac{-Z_2}{Z_1}$

$$\boxed{A = \frac{-L_2}{L_1}}$$

→ for freq of oscillations

$$Z_1+Z_2+Z_3 = 0$$

$$j\omega L_1 + j\omega L_2 - \frac{j}{\omega C} = 0$$

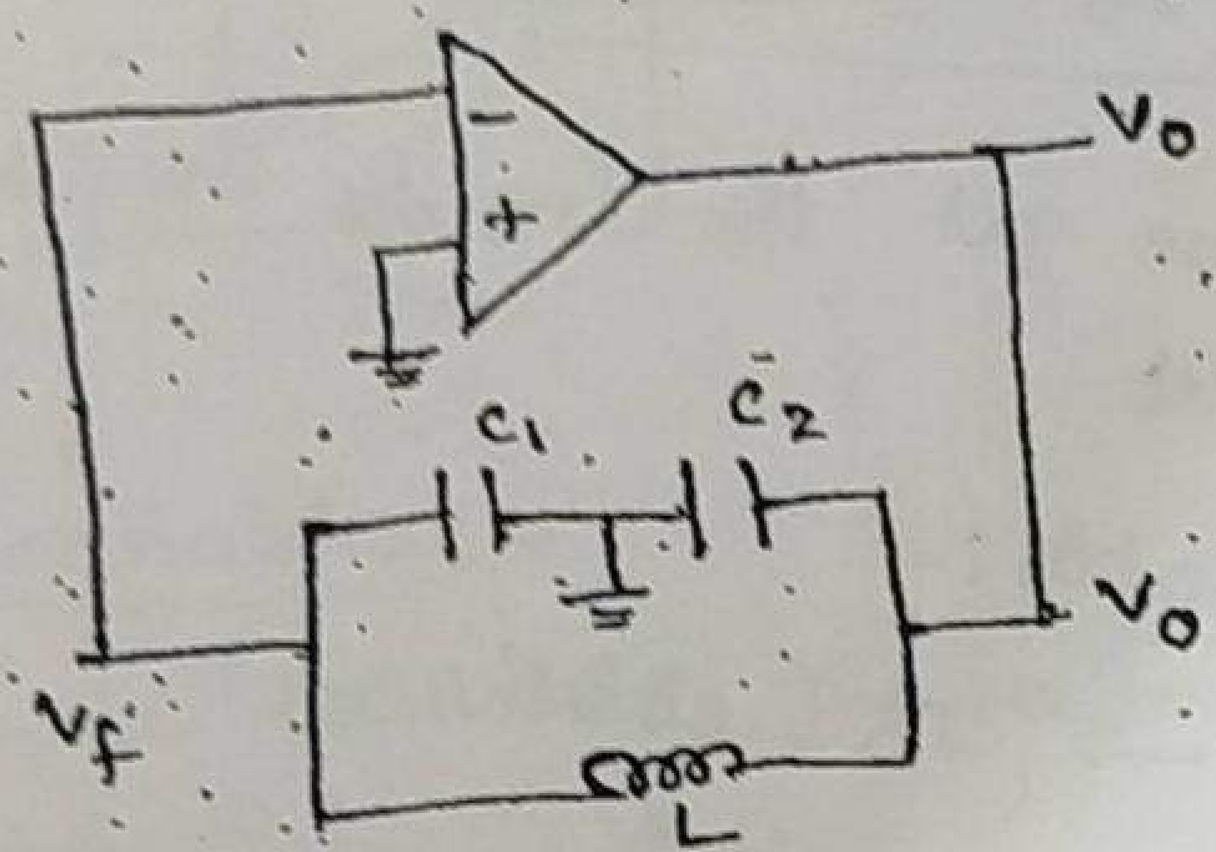
$$\cancel{j}\omega[L_1+L_2] = \frac{\cancel{j}}{\omega C} \qquad \omega^2 = \frac{1}{(L_1+L_2)C} \Rightarrow \omega = \frac{1}{\sqrt{(L_1+L_2)C}}$$

2. Colpitt's oscillator :-

Z_1 & Z_2 → capacitors

Z_3 → Inductor

$$Z_1 = \frac{1}{j\omega C_1}, \quad Z_2 = \frac{1}{j\omega C_2} \quad \& \quad Z_3 = j\omega L$$



→ The feed back factor, $\beta = \frac{-Z_1}{Z_2}$

$$\beta = -\frac{\frac{1}{j\omega C_1}}{\frac{1}{j\omega C_2}} = -\frac{\cancel{j\omega} C_2}{\cancel{j\omega} C_1} = \frac{-C_2}{C_1}$$

$$\boxed{\beta = \frac{-C_2}{C_1}} \quad \boxed{C_1 > C_2}$$

→ The gain of the Amp, $A = \frac{1}{\beta}$

$$\boxed{A = \frac{-C_1}{C_2}}$$

→ for freq. of oscillations,

$$Z_1 + Z_2 + Z_3 = 0$$

$$\frac{-j}{\omega C_1} - \frac{j}{\omega C_2} + j\omega L = 0$$

$$\frac{-j}{\omega}\left[\frac{1}{C_1} + \frac{1}{C_2}\right] + j\omega L = 0$$

$$\cancel{j}\omega L = \frac{\cancel{j}}{\omega}\left[\frac{1}{C_1} + \frac{1}{C_2}\right]$$

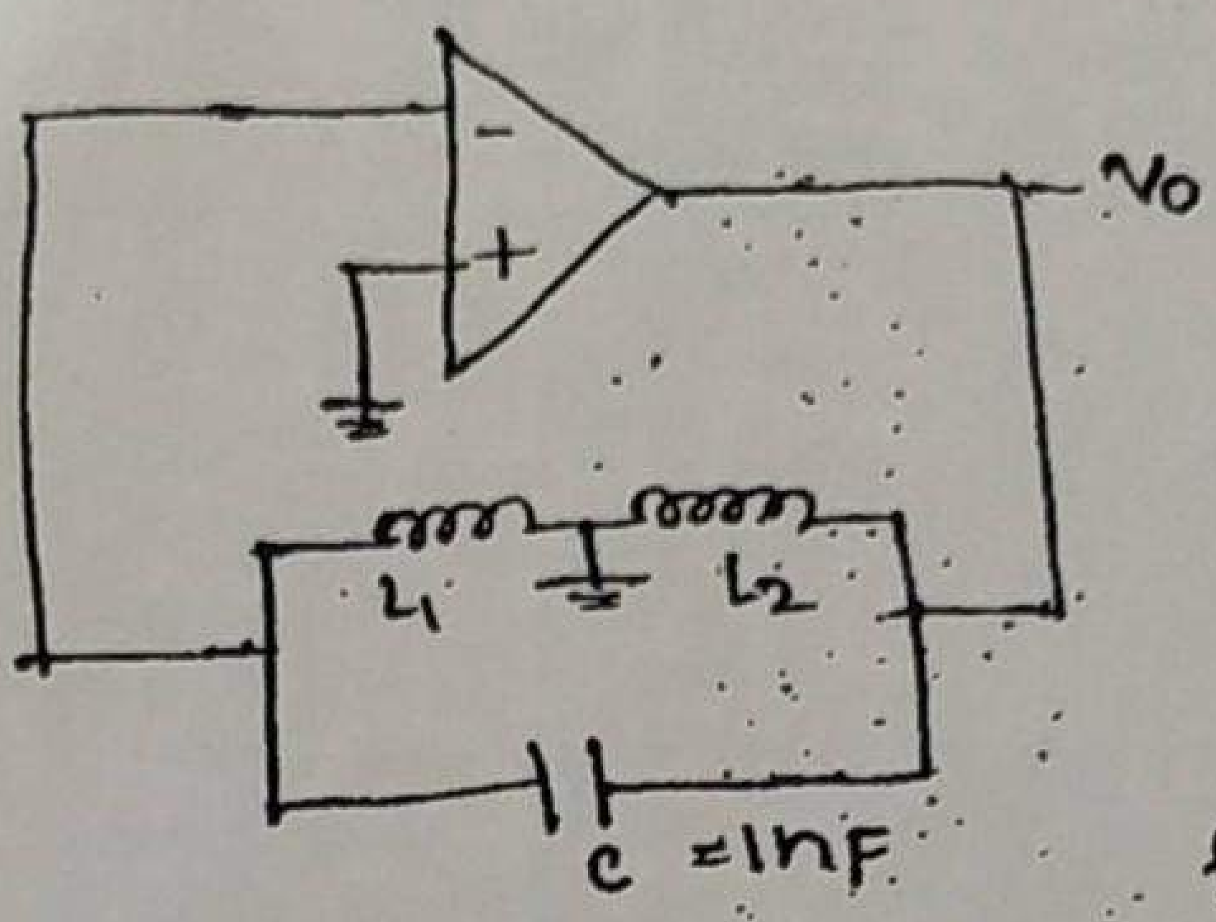
$$\omega^2 L = \left[\frac{C_2 + C_1}{C_1 C_2}\right]$$

$$\omega^2 L = \frac{1}{\left[\frac{C_1 C_2}{C_2 + C_1}\right]}$$

$$\omega = \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

$$f = \frac{1}{2\pi} \times \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{\ldots}\right)}}$$

① The op-amp ckt shown is used to generate undamped oscillation of 60kHz freq calculate the required values of L_1 & L_2, Assume that $|A| = 5$.



$|A| = 5$

$f = 60kHz$

Sol:-

$$|A| = \left|\frac{-L_2}{L_1}\right| = 5$$

$$\therefore \boxed{L_2 = 5L_1}$$

$$f = \frac{1}{2\pi\sqrt{(L_1+L_2).C}}$$

$$\sqrt{(L_1+L_2)C} = \frac{1}{2\pi f}$$

$$(L_1+L_2)C = \frac{1}{4\pi^2 (60k)^2}$$

$$\Rightarrow (L_1+L_2) = \frac{1}{4\pi^2 (6\times k)^2 \times 1n}$$

$$= \frac{1}{4\pi^2 36\times10^{-1}}$$

$$L_1+L_2 = 7.03mH$$

$$L_1+5L_1 = 7.03mH$$

$$6L_1 = 7.03mH$$

$$\boxed{L_1 = \frac{7.03}{6} mH}$$

$$\boxed{L_2 = \frac{5}{6} \times 7.03mH}$$